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The next generation Front-End Controller for the Phase-I Upgrade of the CMS Hadron Calorimeters

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Abstract: The ngFEC (next generation Front-End Controller) is the system responsible for slow and fast control within the Phase-I Upgrade of the CMS Hadron Calorimeters. It is based on the FC7, a μTCA compatible Advanced Mezzanine Card developed at CERN and built around the Xilinx Kintex®-7 FPGA. The ngFEC decodes the 40.0788 MHz LHC clock and the synchronization signals received from the backplane and distributes them to the front-end electronics through six GBT links. The latency of the fast control signals is fixed across power cycles. Even if the direct link to a front-end module is broken, a redundancy scheme ensures a successful communication using the link to the neighboring front-end module. Thanks to the ngFEC all front-end modules can be remotely programmed using the JTAG standard protocol. The CCM server software interfaces the ngFEC to the Detector Control System which constantly monitors voltages and temperatures on the front-end electronics. This document reviews the characteristics and the development status of the ngFEC.

Keywords: Detector control systems (detector and experiment monitoring and slow-control systems, architecture, hardware, algorithms, databases); Control and monitor systems online.

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Contents

1 Introduction

The luminosity upgrade of the Large Hadron Collider (LHC) requires the experiments placed at its interaction points to improve their subsystems in order to preserve physics performance in a harsher operational environment.

The Phase-I Upgrade of the Compact Muon Solenoid (CMS) Detector is outlined in [1]. In particular, the Phase-I Upgrade of the CMS Hadroninc Caloremeter (HCAL) [2] is designed to obtain improved performance with large numbers of pileup events by an increased depth-segmentation and new capabilities for anomalous background rejection. The current hybrid photodiodes installed in the HCAL Barrel (HB) and EndCap (HE) will be replaced by silicon photomultipliers which guarantee a higher signal-to-noise ratio. The single-channel phototubes of the Forward Hadron Calorimeter (HF) will be replaced by multi-anode phototubes operated in a dual-anode configuration. The readout electronics will also be replaced by new charge-integrating ADCs with an integrated TDC. The upgraded raw data rate from the front-end will be increased to 4.8 Gbps.

In order to meet the more demanding requirements coming from the new front-end electronics, the HCAL control system is also going to be upgraded by replacing the VME [3] to the μTCA [4] standard and by replacing/redesigning software and firmware which will add new capabilities and improve its reliability and performance.

The ngFEC (next generation Front-End Control) system distributes the LHC clock to the front-end and manages the control link between the front-end modules and the CMS Detector Control System. Each ngFEC μTCA crate consists of an AMC13 board [5], a μTCA carrier hub (MCH), two redundant power supplies and up to twelve FC7 (FMC carrier - Xilinx Series 7) boards [6]. The AMC13 recovers the LHC clock from the Trigger Timing and Control (TTC) system and sends it to the FC7s through the backplane. The Crate Control Module (CCM) server forms the slow commands and sends them to the FC7s through an Ethernet connection to the MCH.

In this document, Sec. 2 reviews the latest design of the ngFEC system. The results of the radiation tolerance test [7] performed on the Phase-I Upgrade HCAL electronics at the CHARM facility [8] are reported in Sec. 3. The ngFEC status, the installation plan and conclusions are presented in Sec. 4.

2 The next generation Front-End Controller

The ngFEC is the system responsible for the slow and fast control of the Phase-I upgrade of the CMS hadron caloremeters. The ngFEC will be located in the CMS counting room and it was developed to meet the following requirements [2]:

- ability to receive fast control signals from the present TTC system and flexibility to accommodate its future developments;
- ability to distribute TTC signals identically to all front-end crates within each HCAL partition;
- ability to merge fast control and slow control over the same bidirectional optical link used to communicate with the front-end;
- maintain a fixed latency of the fast control signals across power cycles and across identical ngFEC channels;
- ability to make use of the front-end redundancy scheme.

An earlier implementation of the ngFEC has been documented in [9]. Since then, the GLIB board [10] has been replaced with the more powerful FC7. The FC7 was developed at CERN and it is a flexible, μTCA compatible AMC for generic data acquisition/control applications built around the Xilinx Kintex®-7 FPGA [11].

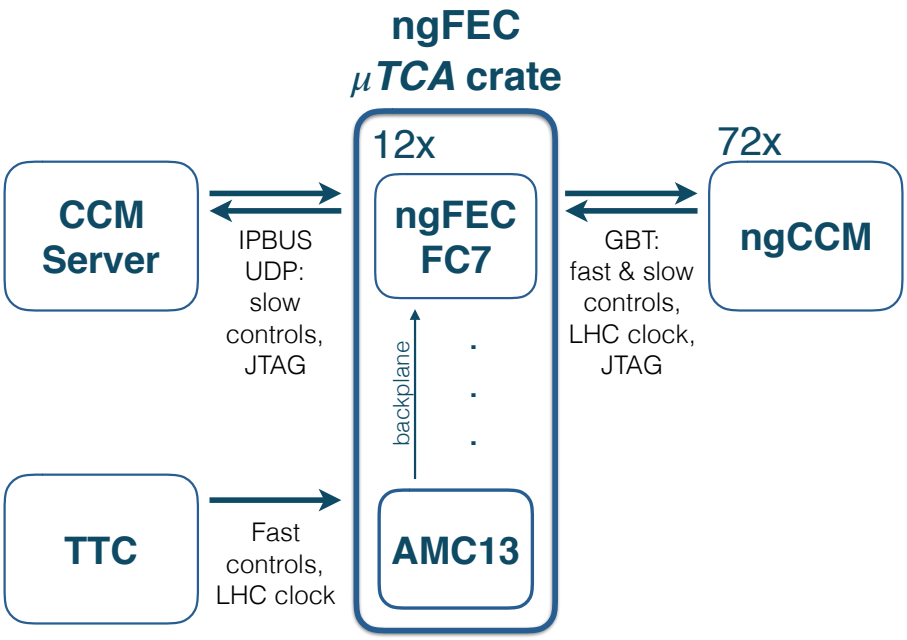

Figure 1. Block diagram of the ngFEC system.

The general layout of the upgraded HCAL control system is shown in Fig. 1. The LHC clock and the fast controls are delivered by the TTC system to the AMC13 board in the ngFEC crate through an optical link. The AMC13, located in the secondary MCH slot, recovers the TTC signals

and distributes them to the ngFEC boards through the backplane exploiting its privileged position within the μTCA crate. In this option, the TTC transmission through the backplane is done through standard I/O buffers and not through SerDes, and this ensures that no latency variations are added to the TTC in this part of the system.

The CCM Server configures the front-end modules, reads the debugging and sensor information (temperature, voltage, etc) and drives the manual controls like reset signals. The CCM Server forms slow control commands and sends them to the ngFECs through the IPBUS protocol [12] as required by the CMS Upgrade Working Group. The commands are stored in 96 kb dual port RAM blocks, which allows the CCM server to issue several commands at the same time reducing the effect of the Ethernet connection latency.

The ngFEC communicates with the next generation Crate Control Module (ngCCM) [13, 14] via GBT protocol [15, 16] through fiber connections.The implemented GBT protocol uses the so-called "GBT-Frame" error detection with the Reed-Solomon (RS) forward error corrections, which allows to correct up to 16 consecutive bit errors ensuring a reliable communication at 4.8 Gbps. In the 84-bits GBT word, one bit is reserved for each I^2C master and all the masters share the same I^2C clock. This allows to maintain a simultaneous and independent 100 KHz communication with each I^2C slave merging fast and slow controls on the same link. Furthermore, the ngFEC is now able to remotely program the Igloo2 [17] FPGAs on the QIE and on the ngCCM boards using the standard JTAG protocol [18].

A block diagram of a single I^2C/JTAG line for the ngFEC-FC7 is outlined in Fig. 2. Each ngFEC can drive up to seven control links to just as many front-end crates.

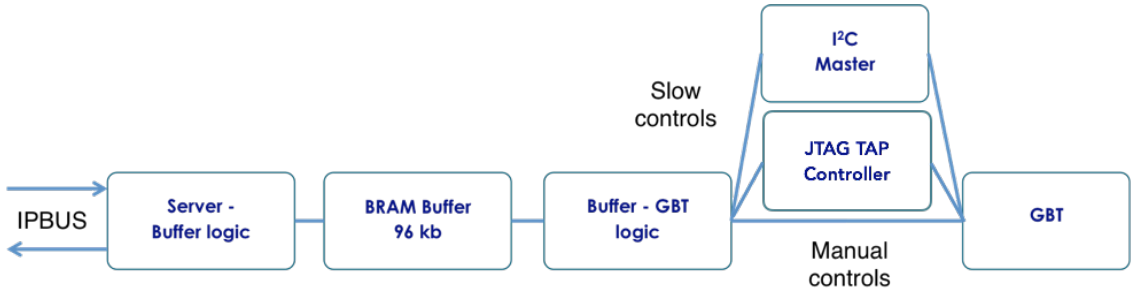

Figure 2. Block diagram of a single I^2C/JTAG line for the ngFEC-FC7.

2.1 The control link error detection module

The communication between back-end and front-end modules must be reliable to ensure continuous operation and monitoring. For this purpose, in addition to the RS forward error correction module contained in the GBT protocol, a bit error rate (BER) detection module was designed and implemented on both side of the link to check the communication quality.

The BER detection module adopted by both ngFEC and ngCCM, consists of a Pseudo-Random Binary Sequence (PRBS) generator and a generic error detection module. The PRBS implementation for HF (HB/HE) generates a 23(20)-bit sequence which is included in the payload of the control link. The received sequence is used by the PRBS module to generate the expected subsequent sequence under the assumption of an error-free communication. Any difference between the

received and the expected sequence would indicate the presence of a communication error that the RS algorithm was not able to correct.

The BER detection module is one of the key ingredients that allowed to precisely assess the quality of the ngFEC-ngCCM bidirectional link during the radiation tolerance test of the front-end electronics as described in the following section.

3 Irradiation test at CHARM

The CMS HCAL group carried out a radiation tolerance test [7] for the Phase-I Upgrade of the HF, HE and HB front-end electronics from October the 21^{st} to the 28^{th}, 2015 at the CHARM facility [8] located at CERN. At CHARM, bunches from the 24 GeV proton beam of the CERN Proton Synchrotron are sent on one of three different targets (aluminum sieve, solid aluminum, and solid copper) to create a mixed radiation environment.

Two systems were irradiated: the former consisting of one HF crate containing two HF QIE cards and one HF-ngCCM card; the latter consisting of one HE readout module containing two HE QIE cards. Both HF and HE front-end electronics employ radiation tolerant FPGAs such as Igloo2 [17] and ProASIC3(L) [19] from Microsemi. Together, the two irradiated systems feature fifteen 5 Gbps lines and one 4.8 Gbps bidirectional line. Only the HF control-link stability test is discussed in what follows, further tests on HF and HE QIE cards can be found in [7].

The back-end electronics used for the test is similar to the back-end electronics for the Phase-I Upgrade of CMS HCAL described above. The back-end electronics was located in an area at CHARM without ionizing radiation. An AMC13 was used to receive the input clock at the nominal LHC clock frequency of 40.0788 MHz and distribute it to an ngFEC sitting in the same μTCA crate. The crate was connected to a computer running the CCM server and crate monitoring software. The ngFEC was used to control the front-end electronics. The serial bidirectional link between the ngFEC and the HF-ngCCM was established through single mode optical fibers with an SFP+ FTLX1370W3BTL transceiver from Finisar on the ngFEC side and a Single Mode VersaLink Transceiver (VTRx) from CERN on the HF-ngCCM side. The GBT with RS error correction was used as communication protocol.

A first run was performed to check the link stability in case the front-end is not exposed to radiation. The system was run under such condition during the whole week preceding the radiation test and no PRBS errors were observed.

During the test at CHARM, a total of seven runs were recorded: three runs were taken using the aluminum sieve target and the remaining four with the copper target, which produces a stronger radiation environment. The number of PRBS errors on the ngCCM→ngFEC link were logged once every two minutes. According to this time resolution, the pattern errors occurred in bursts of maximum 2000 rather than increasing constantly. Figure 3 shows the cross section of PRBS error burst occurrences as calculated from Eq. 3.1:

$$\text{PRBS error cross-section} = \frac{\text{Num. of error bursts}}{\int \mathcal{F}_{HEH}} \tag{3.1}$$

where $\mathcal{F}_{HEH}$ is the flux of charged hadrons with energy greater than 20 GeV. As can be observed in Fig. 3, the PRBS cross section depends on the radiation level, but it does not depend on the integrated dose/charged hadron flux.

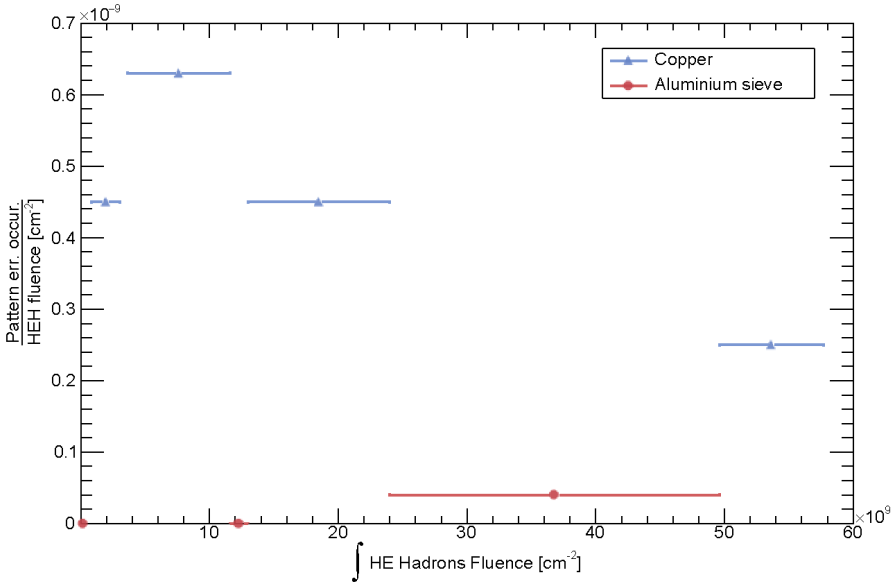

Figure 3. Error cross section as a function of the integrated HEH flux.

As for the ngFEC→ngCCM link, the error detection module did not detect any PRBS error during stable operations.

Is it important to note that the test herein described is the first irradiation test on a readout system that combines a VTRx module and the GBT protocol with the RS error correction.

4 Conclusions

The control system of the CMS HCAL Phase-I upgrade, provided with a modern and powerful hardware, new firmware and software, is faster, more reliable and it is equipped with more functionalities than the current legacy control system.

Each ngFEC FC7 can simultaneously drive fast signals and slow controls to 15 (12) I^2C slaves for each of its six links to the HF (HB/HE) ngCCMs. Furthermore, the ngFEC FC7 exploits the front-end redundant scheme and can remotely program the Igloo2 FPGAs on the front-end electronics via the JTAG protocol, increasing the possibility of recovery from operational failures.

The system has been tested in three test stands (CERN, DESY, and FNAL), in dedicated irradiation tests performed at the CHARM facility, and with real proton-proton collisions at CMS. The installation of the HF and HE subsystem is foreseen during LHC EYETS 2016/17.

Acknowledgments

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