

Progress in Chip Testing

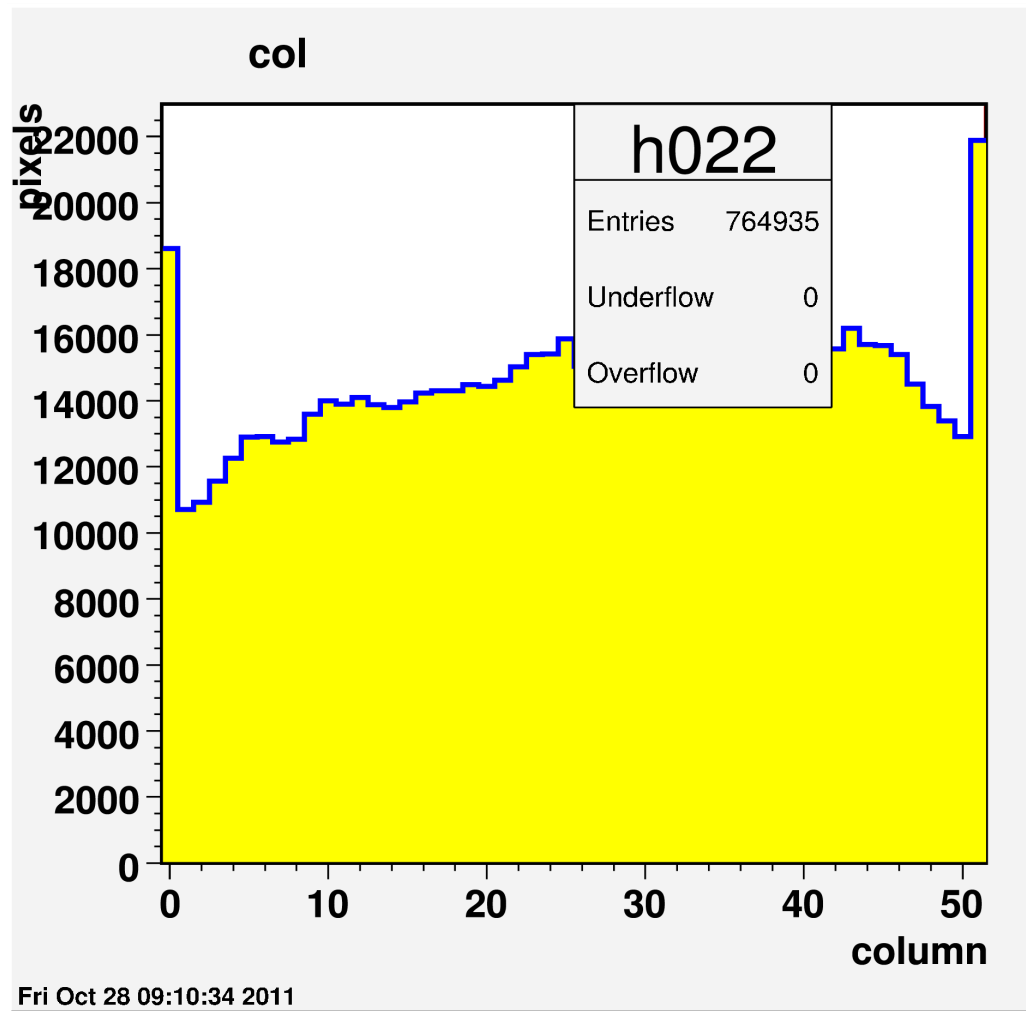
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CMS Tracker Upgrade 01.11.2011

- Double columns
- V scan
- Threshold scan
- UB level
- Data taking eff.
- Bump bonding test

Double Column Issue

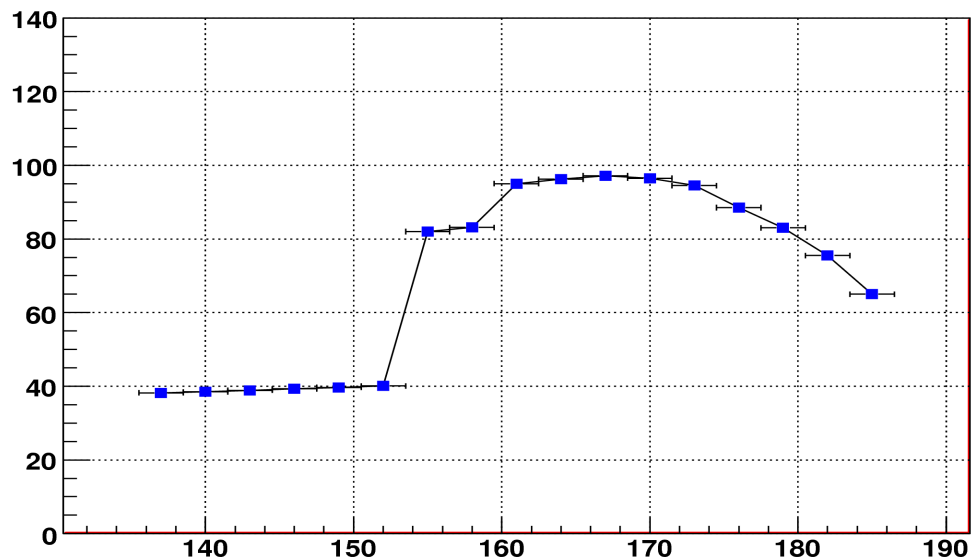


- 2 GeV e+ test beam
- Chip 6 (sensor)

No missing double columns now: solved by adding more time delays into USB data reading procedure.

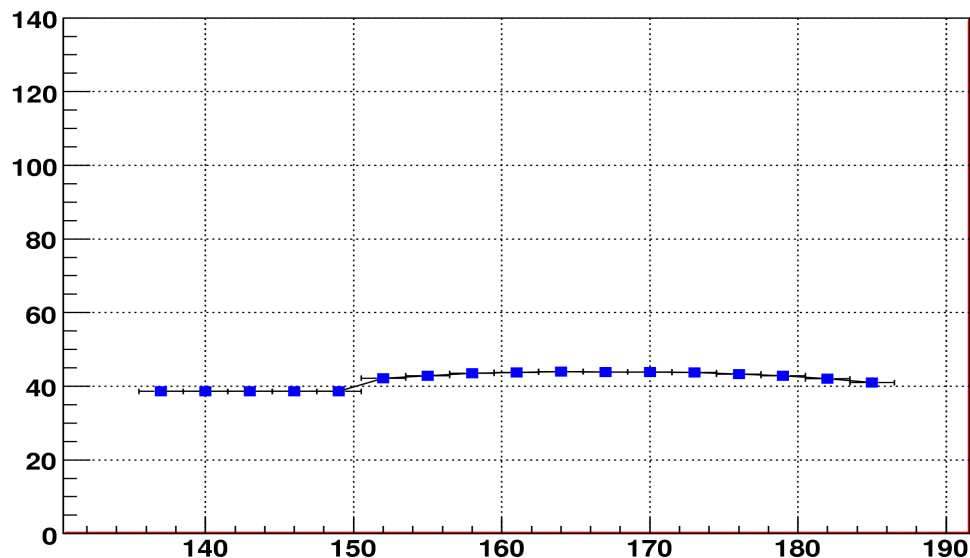
Threshold Scan and Power

Id vs VthrComp



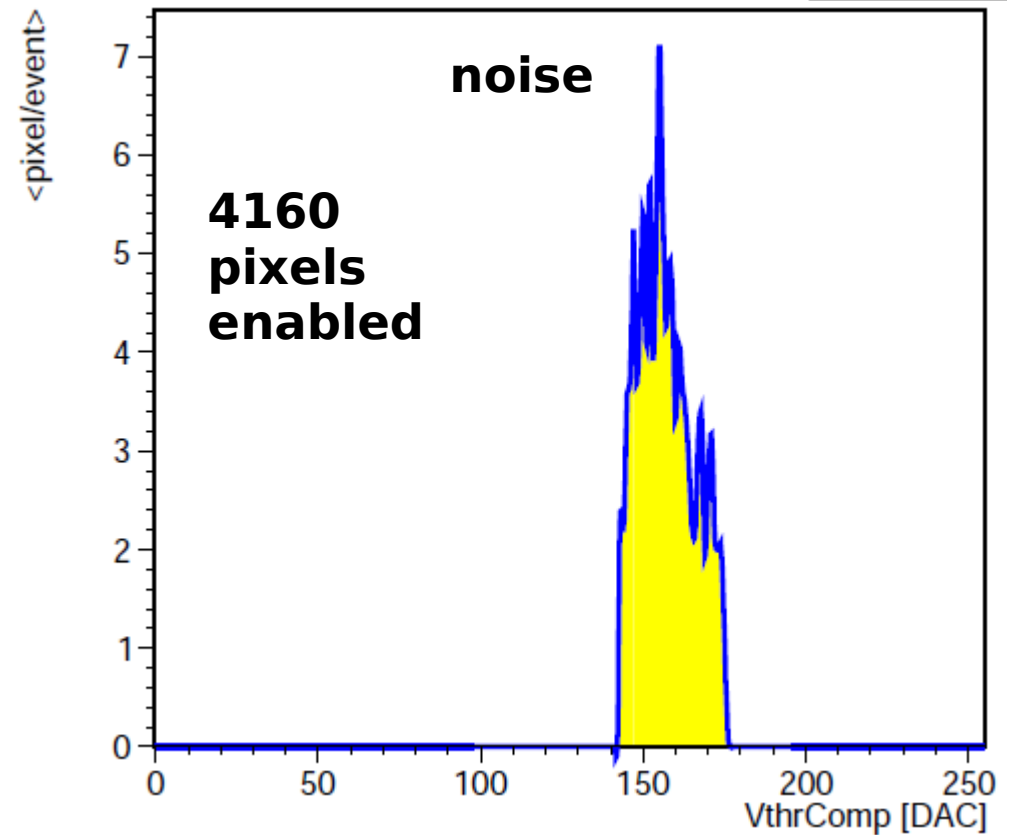
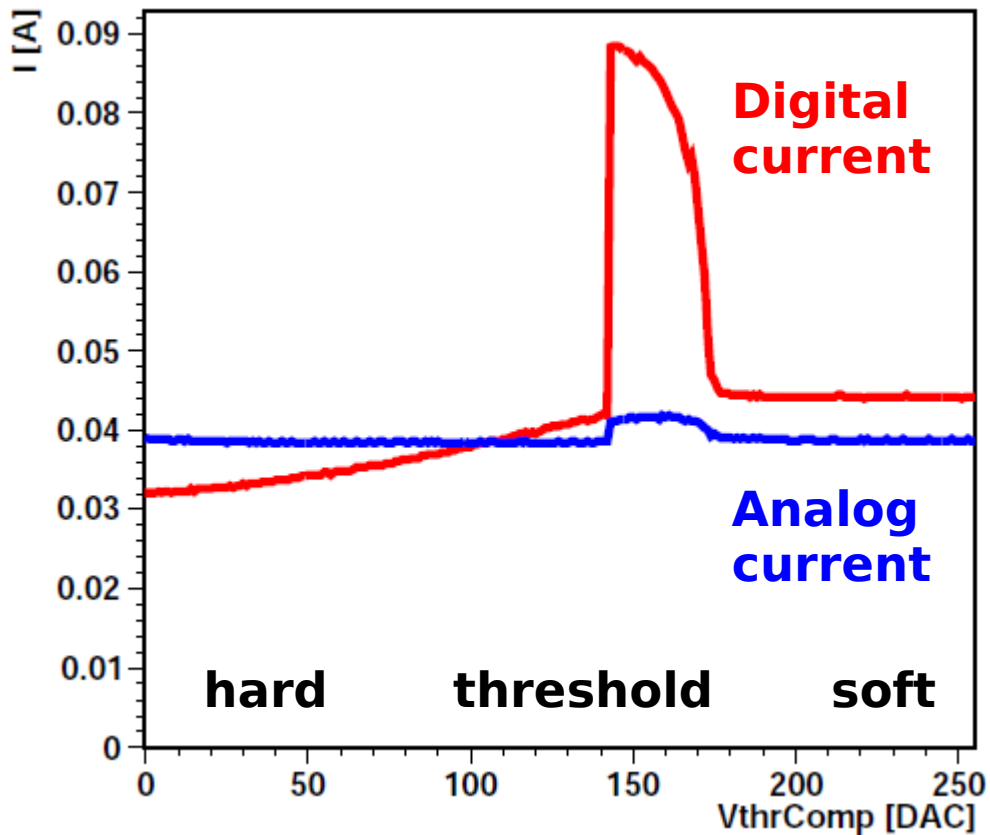
- Chip 2 (no sensor)
- Id (mA) vs VthrComp
- Threshold into noise
- Chip consumes 2.5 times more power at low threshold (high VthrComp)

Ia vs VthrComp



- Chip 2 (no sensor)
- Ia (mA) vs VthrComp
- Small effect at low threshold
- The same trend for Chip 6 (sensor)

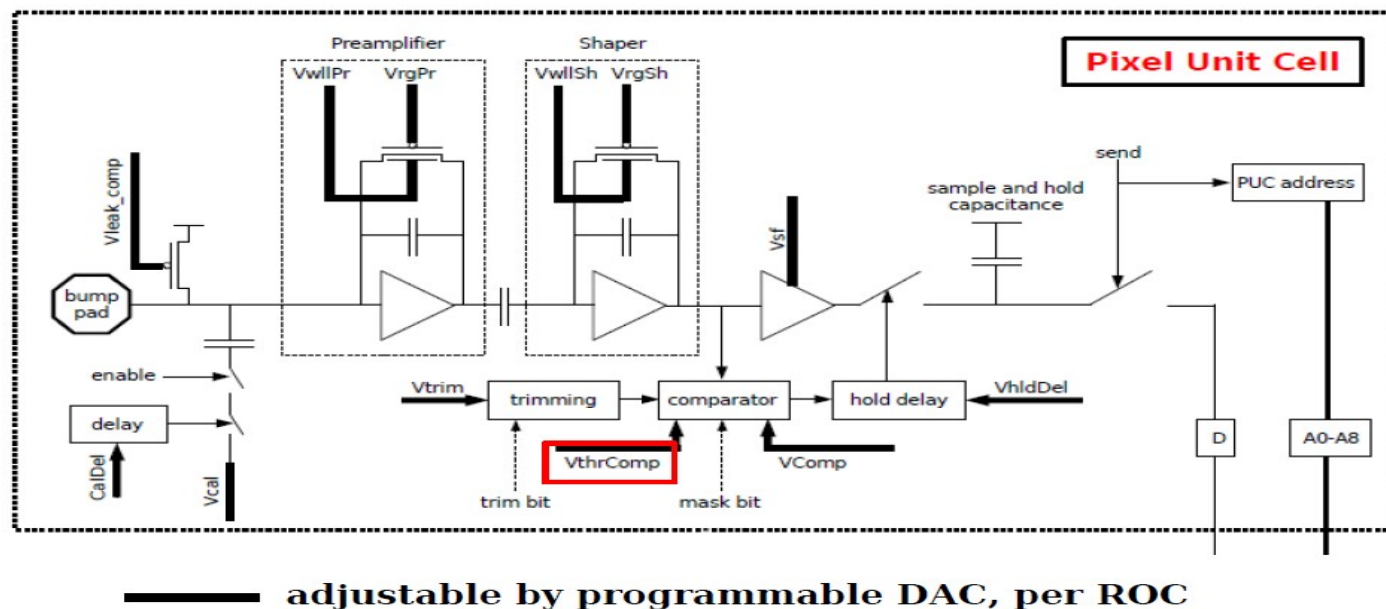
Power and noise



- 40 MHz clock, random trigger
- 6 hits / event = 375 MHz / cm².
- Noise = poor man's high rate test?
- **Digital current depends on occupancy!**

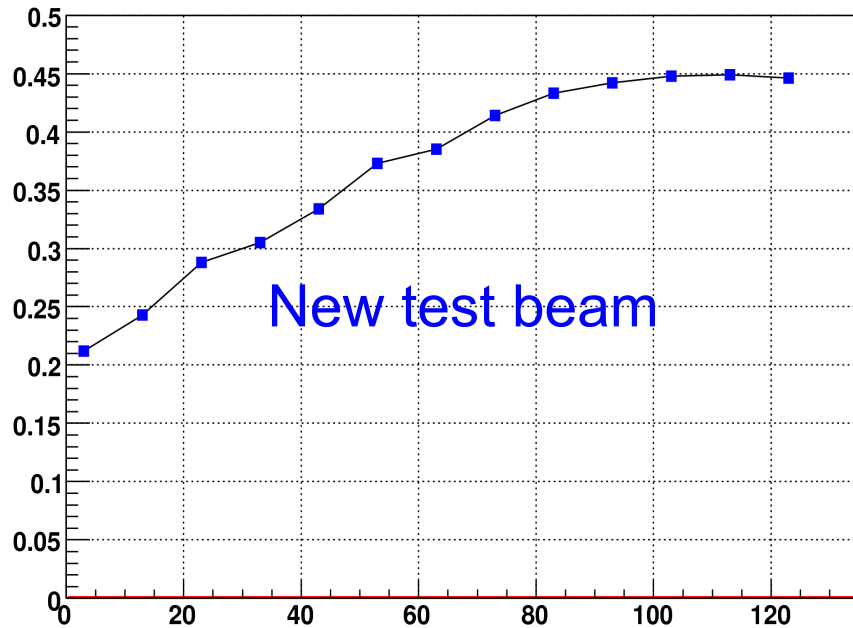
Threshold Scan Procedure

- DESY 2 test beam: 2 GeV e+, 5 kHz scintillator trigger, V_{bias} -90 V
- Chip 6 (sensor), calibrated, trimmed, optimal DAC parameters
- 50 sec runs, 50 - 109 k clusters per run
- Change $V_{thrComp}$ from 3 to 123(optimal) DAC units. Large DAC = soft threshold

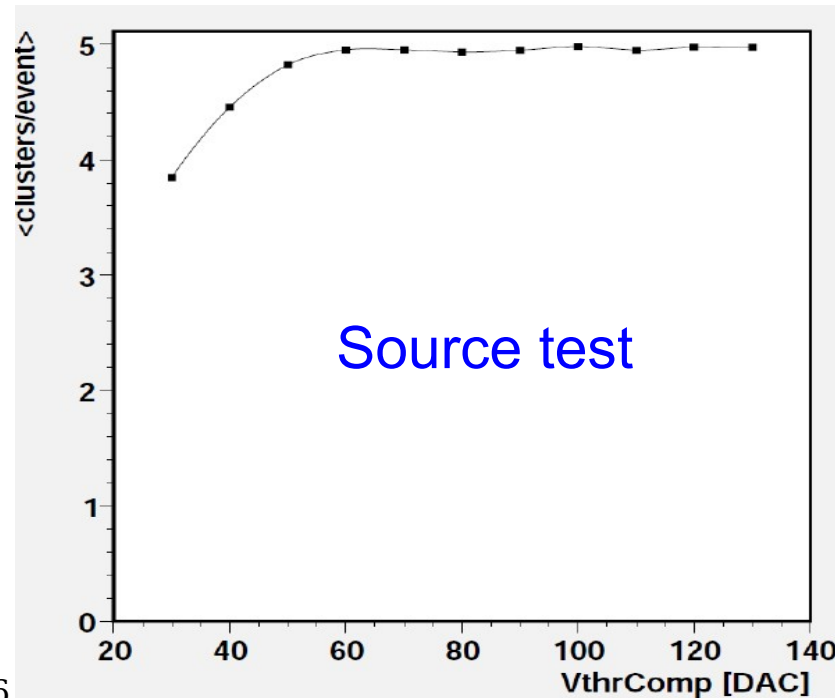
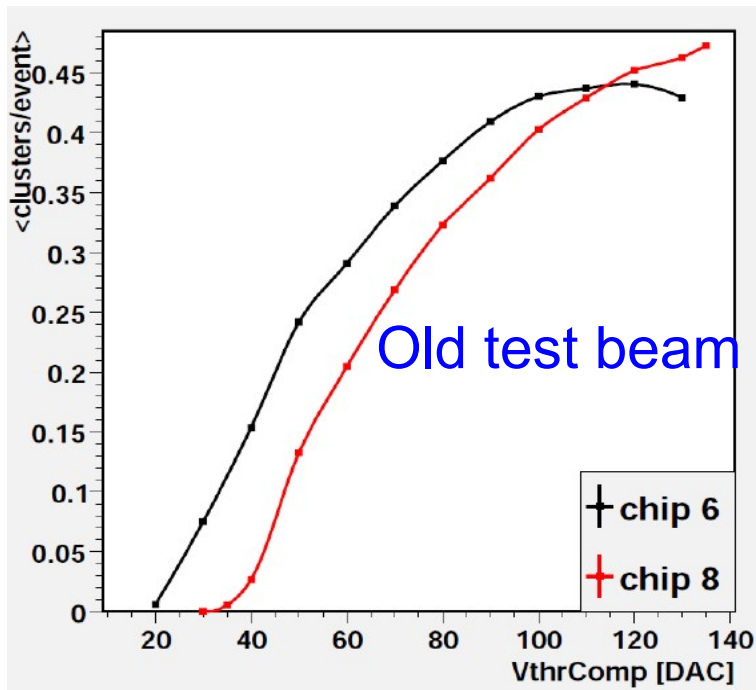


Threshold Scan Results

clusters/event vs VthrComp



- Uniforming of pixel thresholds (trimming) makes an efficiency plateau visible
- More close to source test results now ?



UB Level

- Ultra Black level is used to mark the beginning and the end of the data packet and to separate individual ROC information
- Issue: UB level can not be identified for chips (sensor and no sensor) in TBM mode
- 3d scans: clk (LHC clock), sda (DACs programming), rda (token out signal). Takes 2 hours each, ~2 days in total → no UB level
- TBM DAC 'Dacgain' (UB TBM) and 'Ibias_DAC' (UB ROC to UB TBM) have no effect to UB level
- Report to PSI in December ?

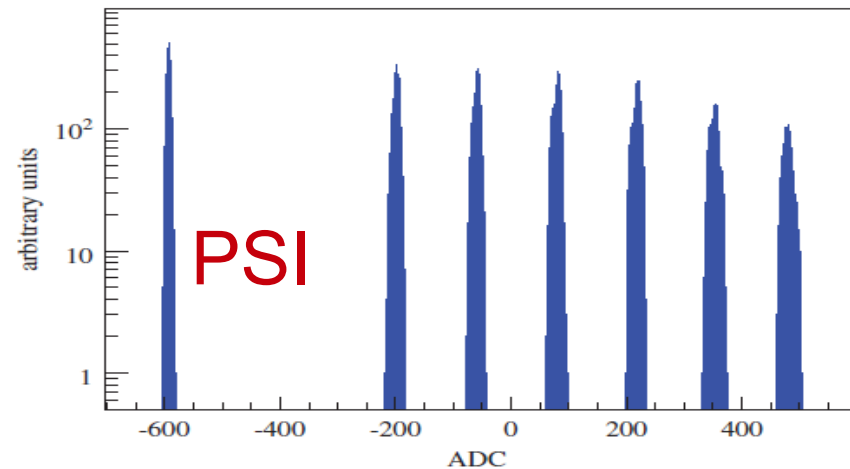
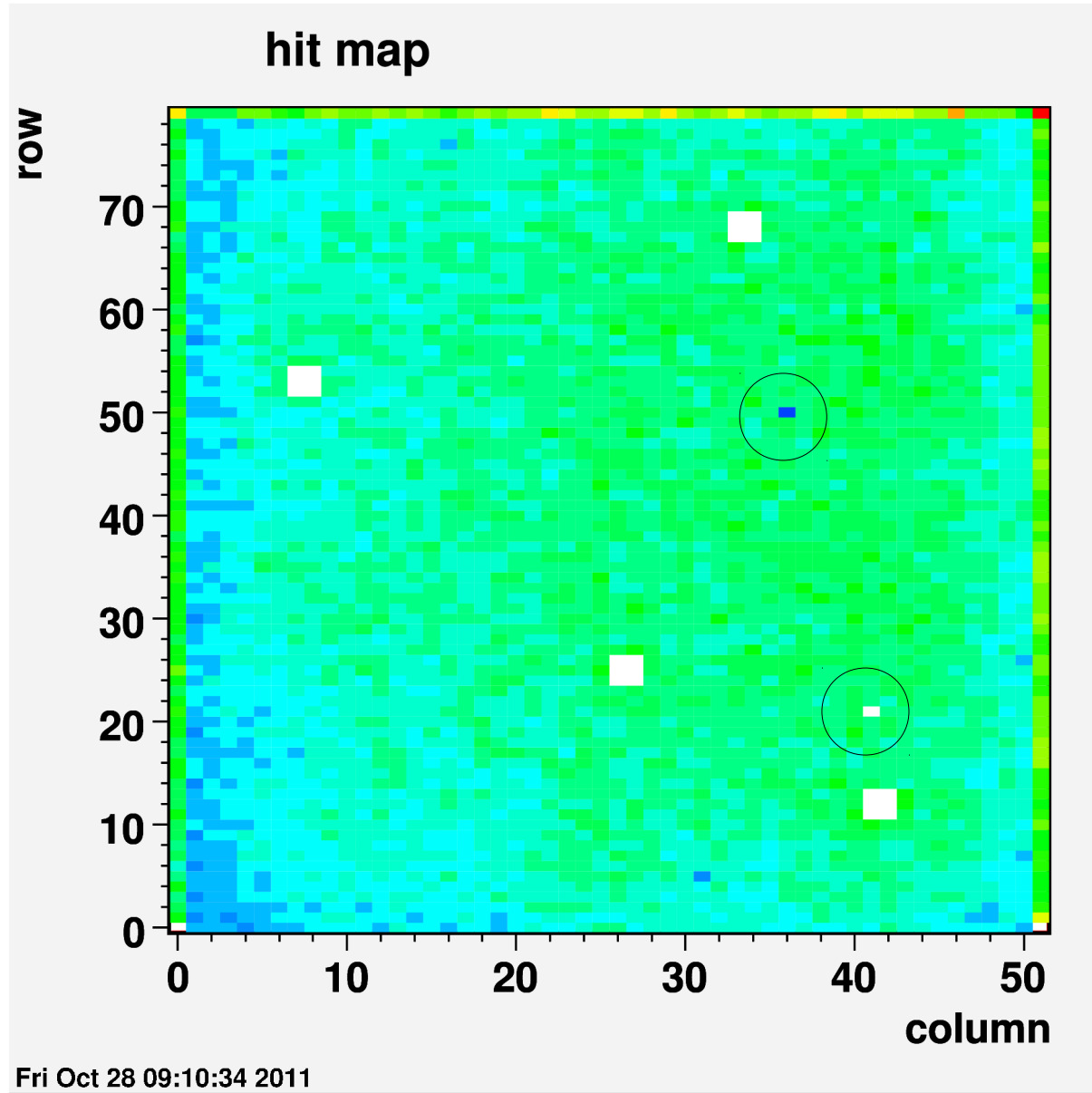


Fig. 3. 'Ultra black' (left most) signal and six levels of the analog signal coded pixels addresses.

DAQ Efficiency

- No corrupted data during data taking! - reported by Daniel 18/10/2011
- Confirmed on test beam, Fri. 21/10/2011
- Reason for past data lost: slow USB, time window was not wide enough for sending of large data blocks
- Solved by reducing of data block size sent via USB from 2^{15} to 10.000
- Result: slightly slower DAQ but 100% efficient data taking

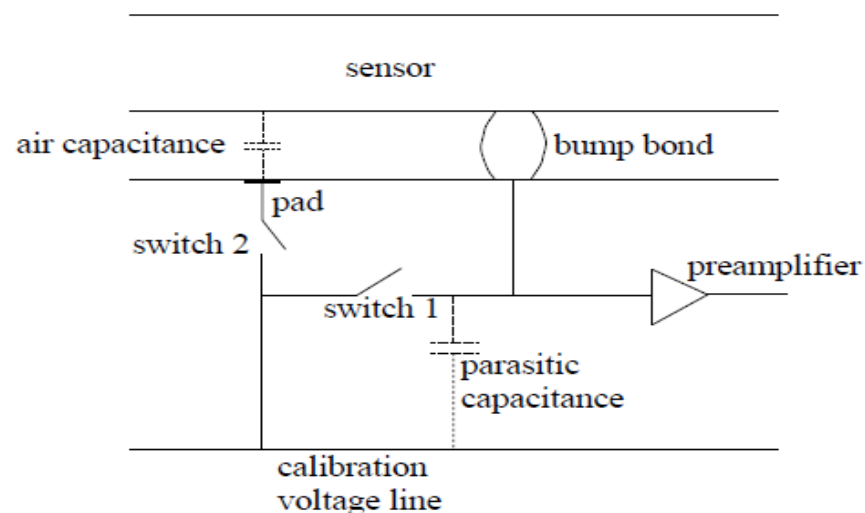
Bump Bonding Test Necessity



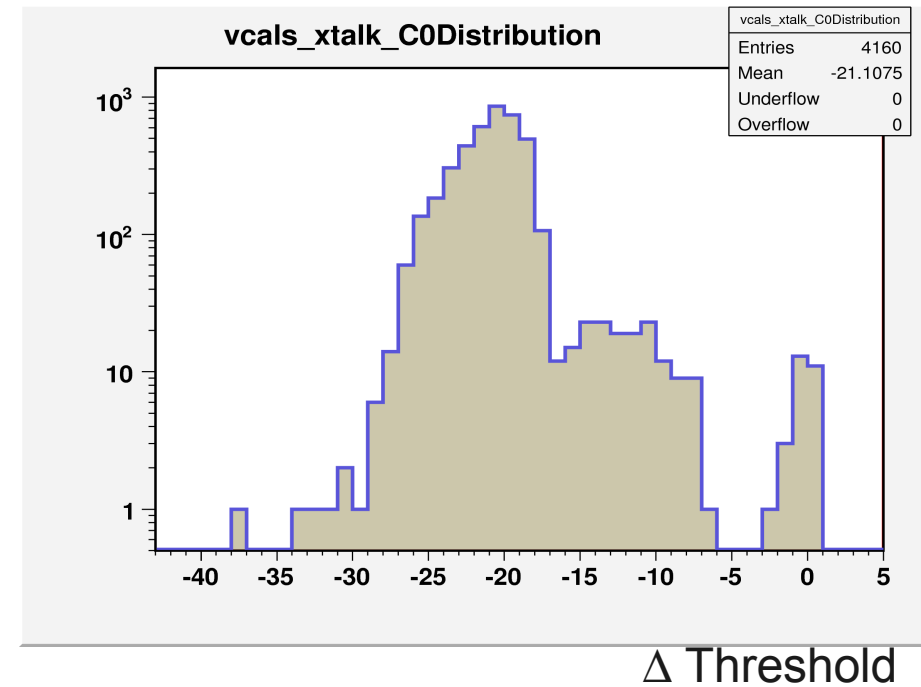
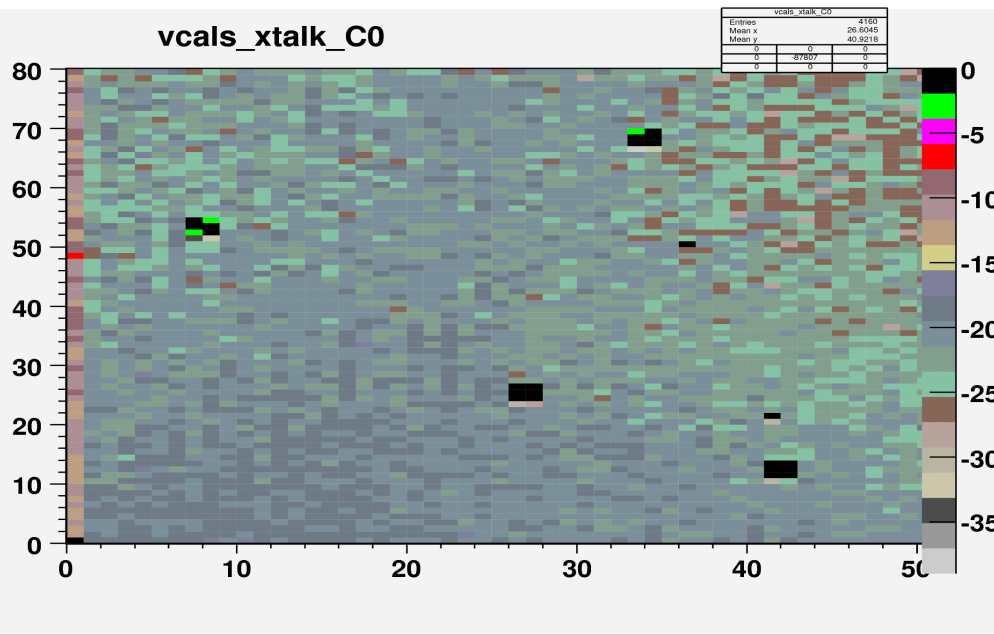
- 2 GeV e+ test beam
- Chip 6 (sensor)
- 2 dead pixels
- 4 dead regions
- Use 'psi46expert' to test bump bonding

Bump Bonding Test Procedure

- Vcal to switch 2 induces a signal in sensor. If bump bond (bb) is present it is seen by preamplifier: missing bb can be identified
- Problem: cross-talk via a parasitic coupling between the calibration voltage line and preamplifier can fake a signal even without bb
- Determine Vcal_Thr2 for the signal injection through the sensor
- Measure Vcal_Thr1 for the parasitic cross-talk (with both switches open)
- $|V_{cal_Thr1} - V_{cal_Thr2}| < 5 \text{ DAC units} \rightarrow$ defect bump bonding



Bump Bonding Test Results

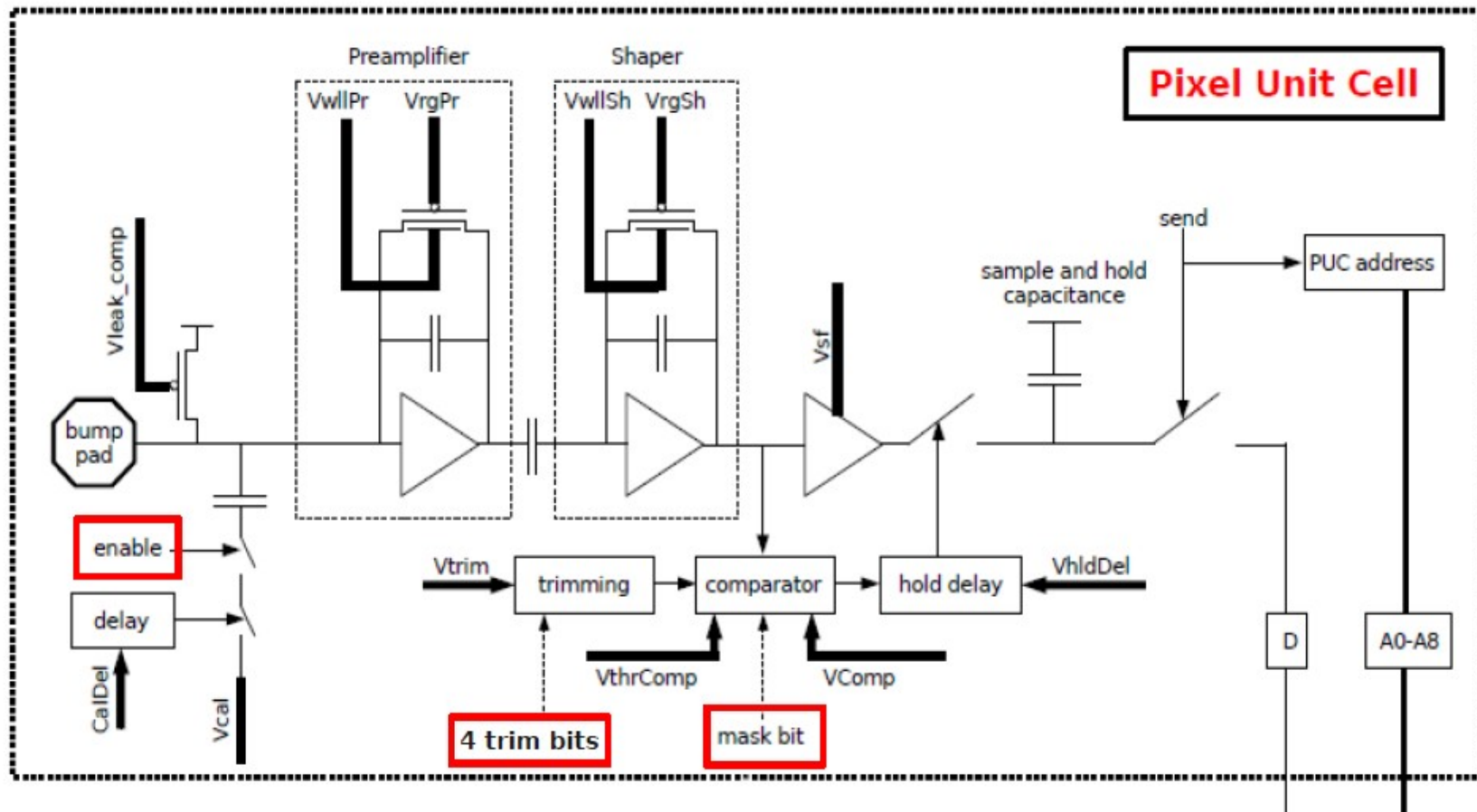


- Threshold difference: expected defects from beam test are correctly identified by 'psi46expert'
- Peak at Δ Threshold ~ -20 \rightarrow good bump bonds. Peak at Δ Threshold ~ 0 \rightarrow bad bump bonds

Summary

- Software problems which produced data loss (big data blocks) or corrupted data (missing dcols) are solved
- V scan shows a high energy consumption for loaded chips
- UB level issue is not solved yet
- New test beam threshold scan after calibration, DAC parameters optimization and threshold trimming shows a need of the procedures. Repeat previous test beam result
- Psi46expert bump bonding test is working after a small software tuning - good for test of bare modules

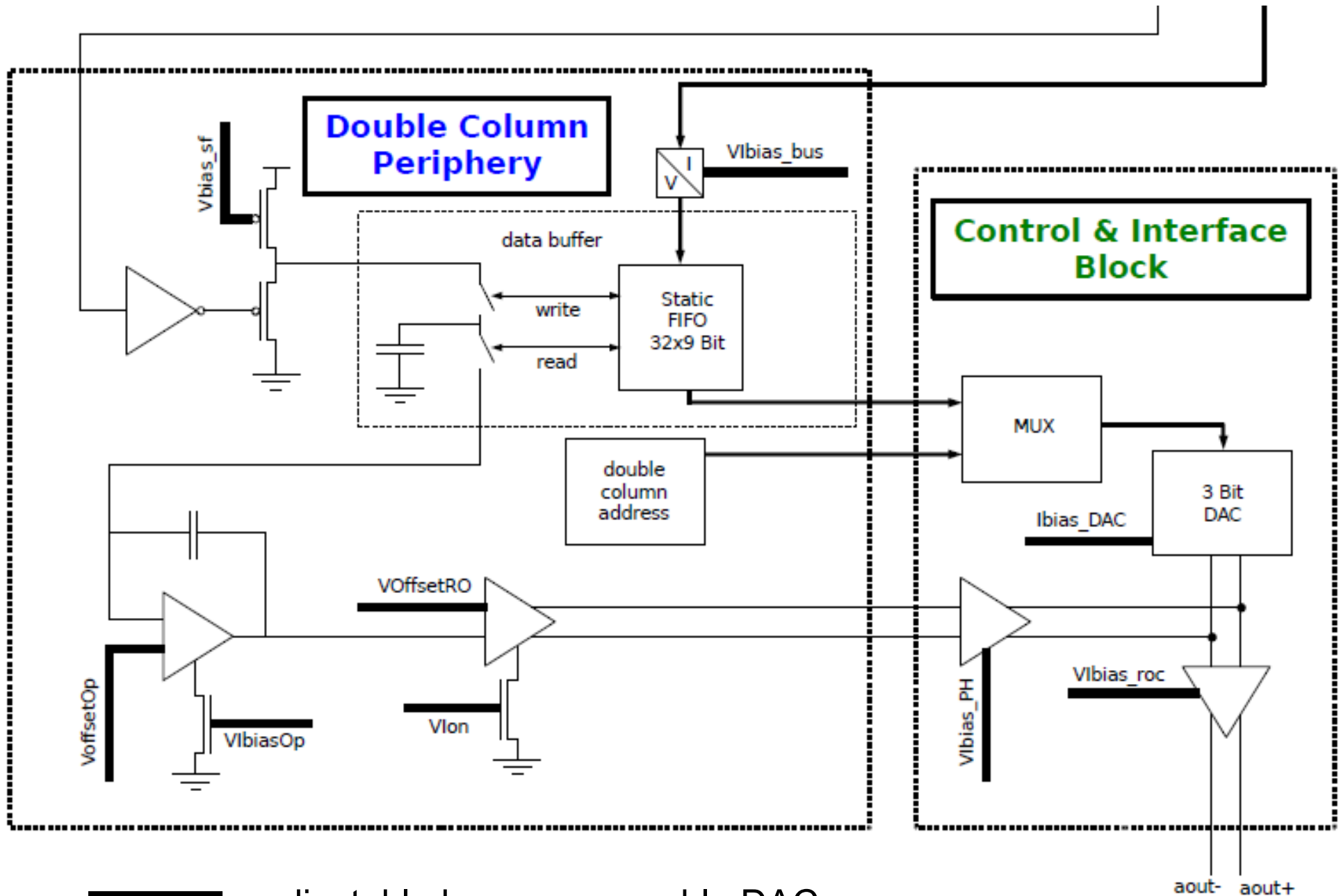
Psi46 Pixel Readout Chip



— adjustable by programmable DAC, per ROC

□ programmable register, per pixel

psi46 pixel readout chip



adjustable by programmable DAC

psi46 DACs

1	Vdig	6	13	VIBias_Bus	30
2	Vana	150	14	Vbias_sf	10
3	Vsf	160	15	Voffset0p	55
4	Vcomp	10	16	VIBias0p	115
5	Vleak_comp	0	17	VOffsetR0	120
6	VrgPr	0	18	VIon	115
7	VwllPr	35	19	VIBias_PH	130
8	VrgSh	0	20	Ibias_DAC	122
9	VwllSh	35	21	VIBias_roc	220
10	VhldDel	130	22	VIColOr	100
11	Vtrim	7	23	Vnpix	0
12	VthrComp	124	24	VSumCol	0
253	CtrlReg	0	25	Vcal	200
254	WBC	20	26	CalDel	125
			27	RangeTemp	0