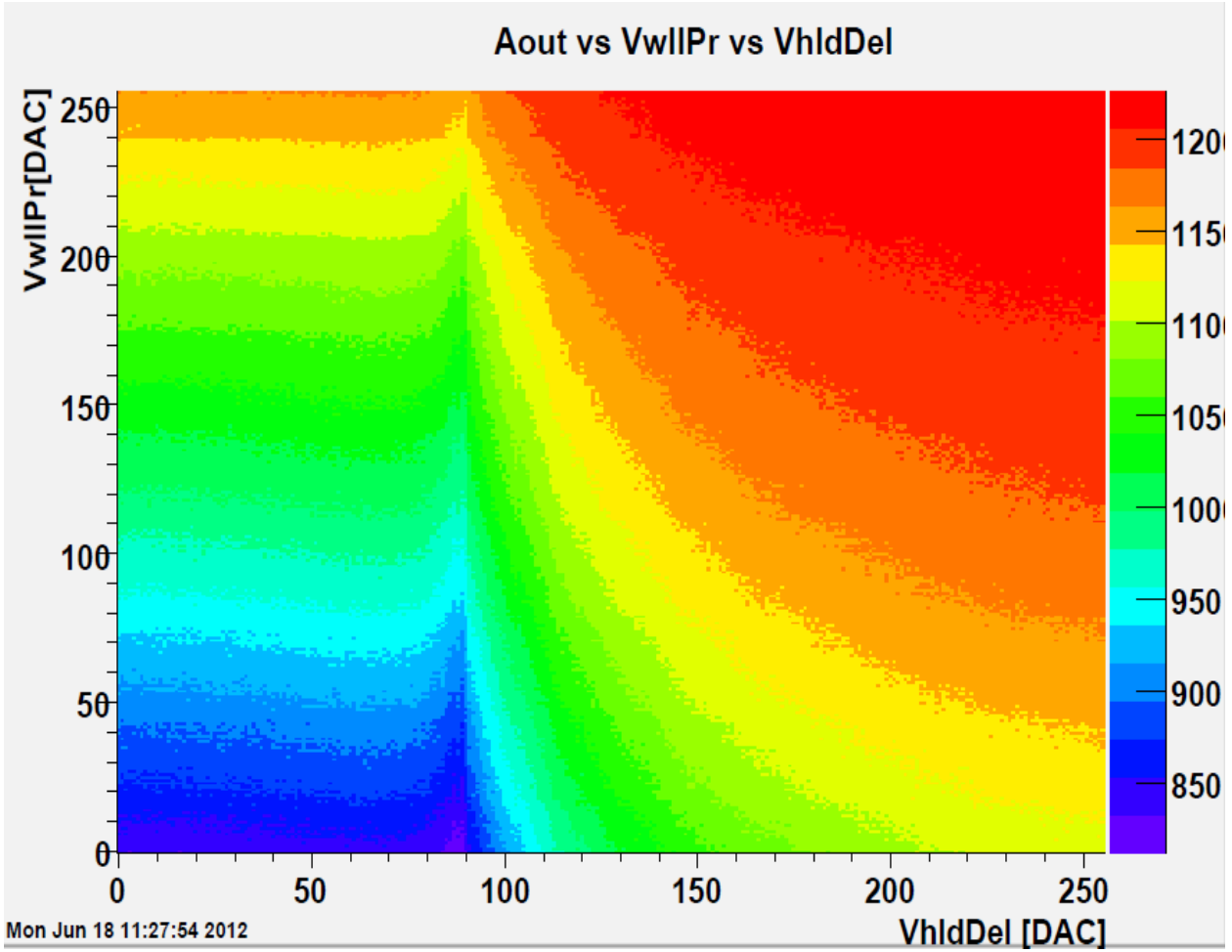
VhldDel scan

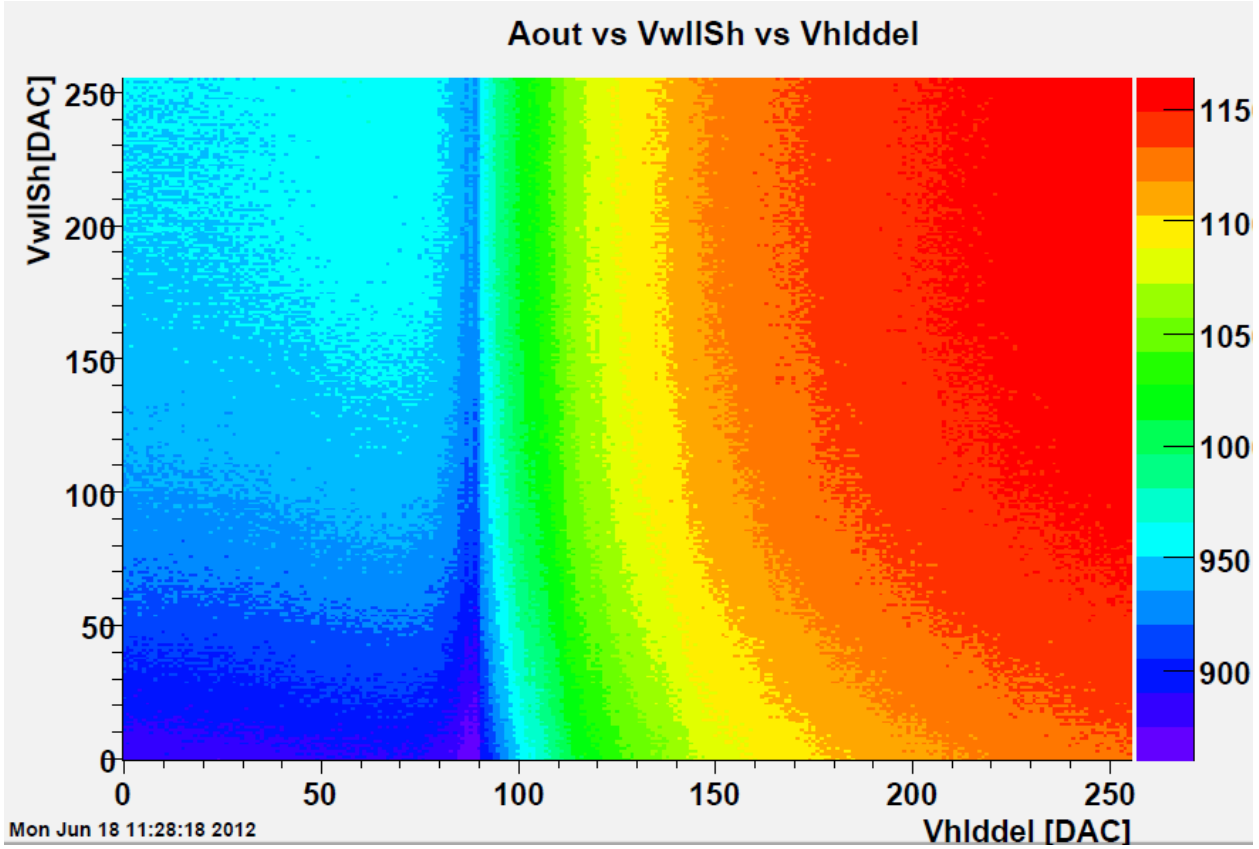
A. Petrukhin, D. Pitzl (DESY)

Chip xdb CtrlReg 4



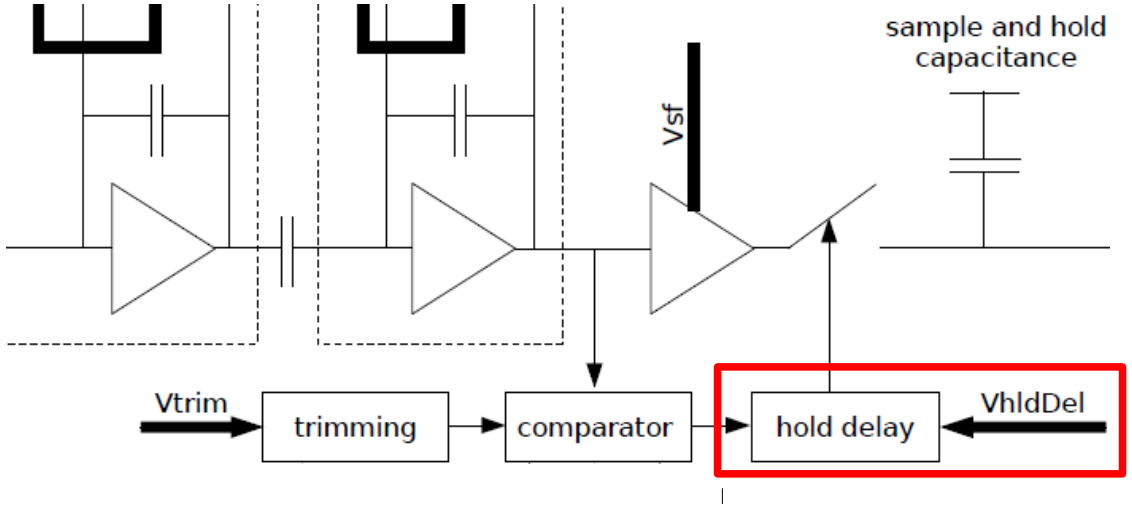
Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=60, VwllSh=60, VhldDel=250, Vcal=200, CtrlReg 4.

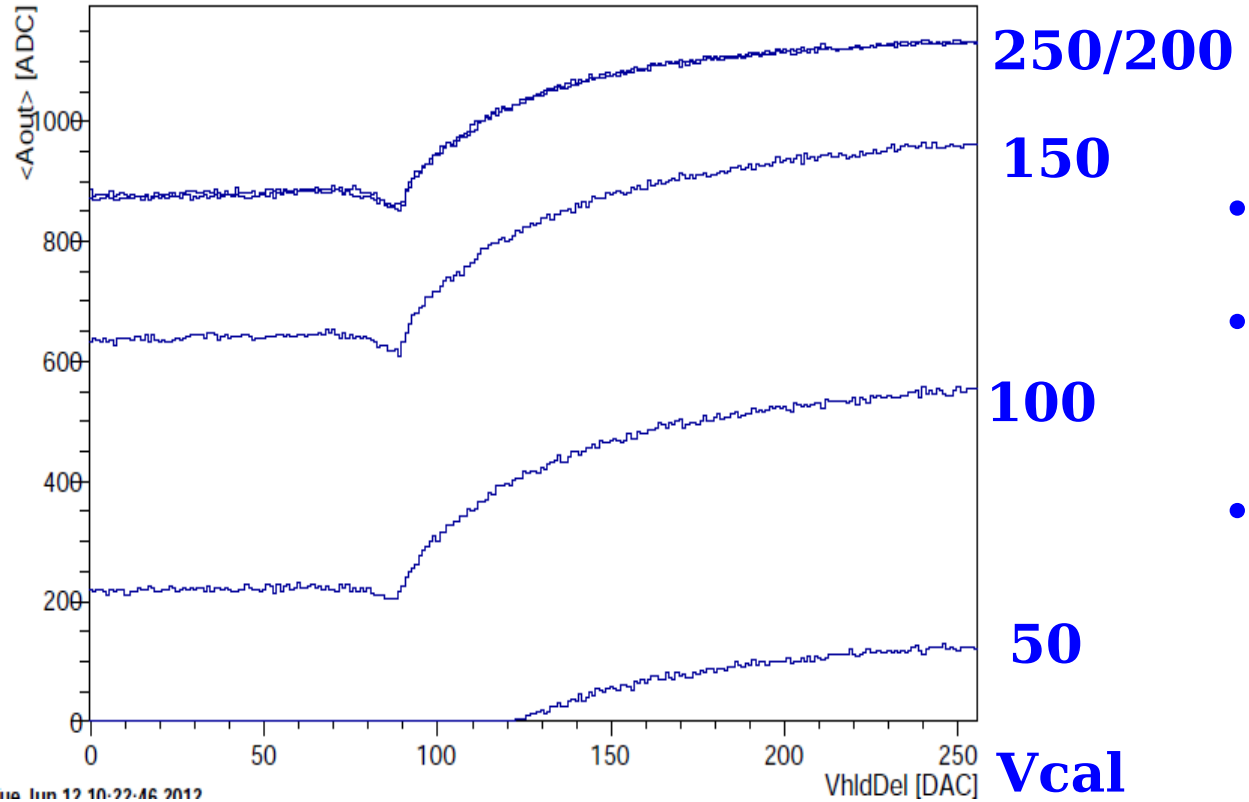
Chip xdb CtrlReg 4



Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=60, VwllSh=60, VhldDel=250, Vcal=200, CtrlReg 4.

Sample and hold timing xdb





250/200

150

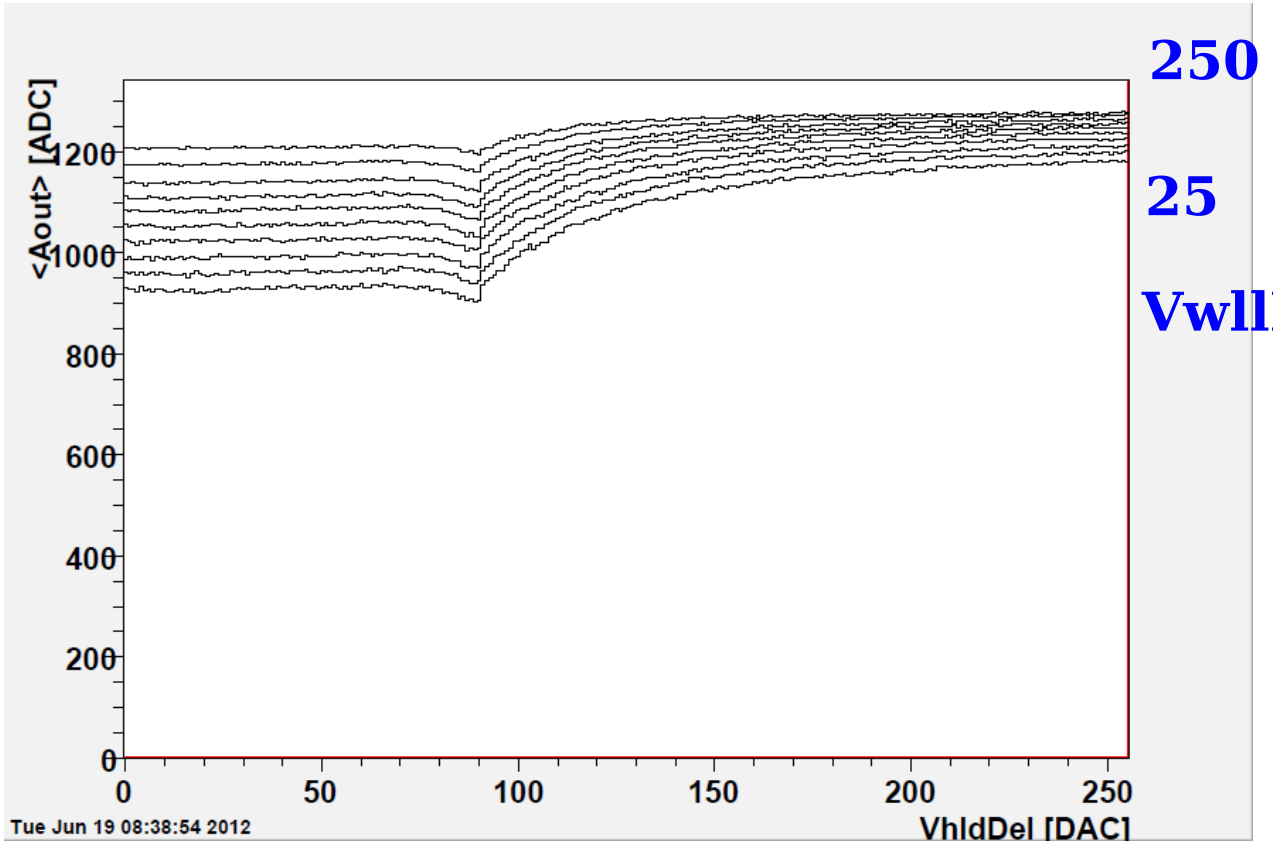
100

50

Vcal

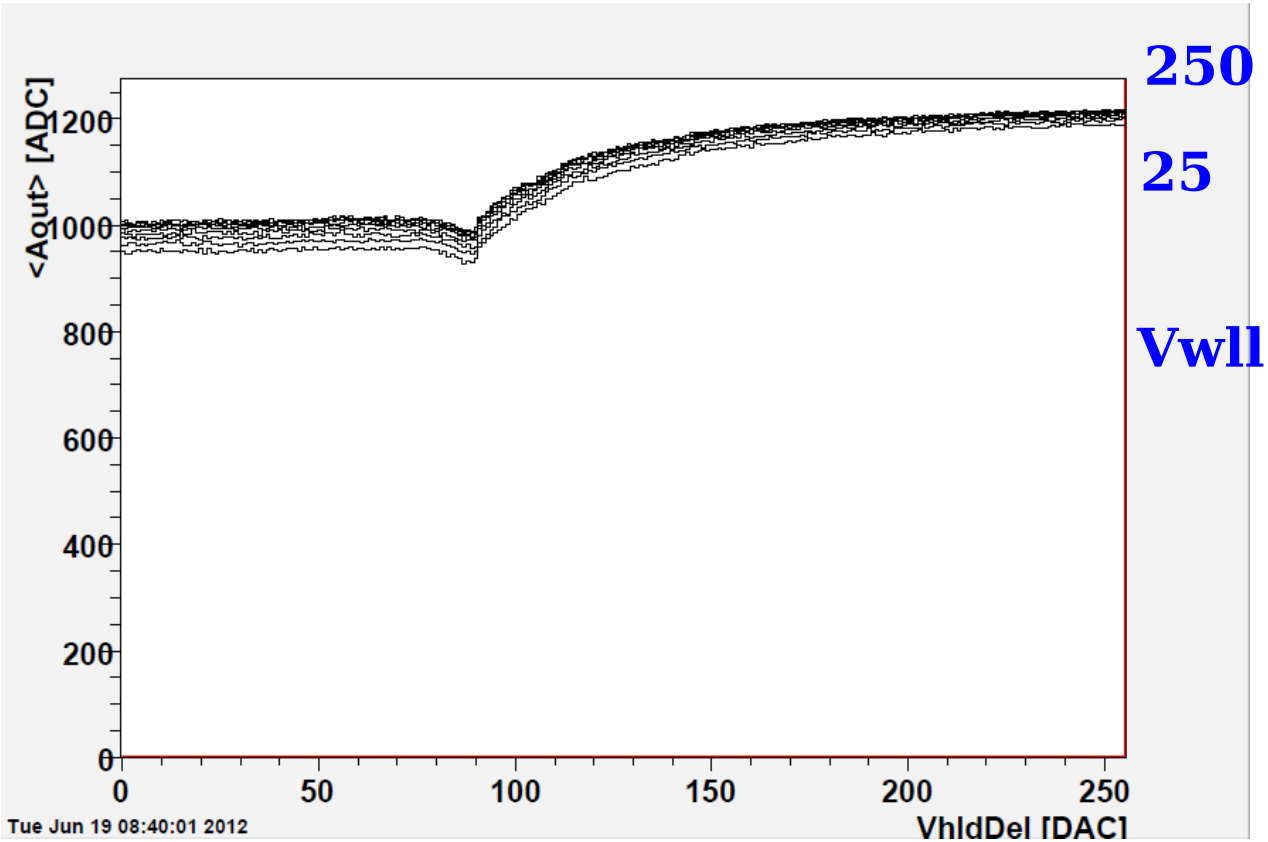
- One pixel, CtrlReg 4
- Change Vcal from 50 to 250
- VhldDel= 250 is a compromise ?

Sample and hold timing xdb



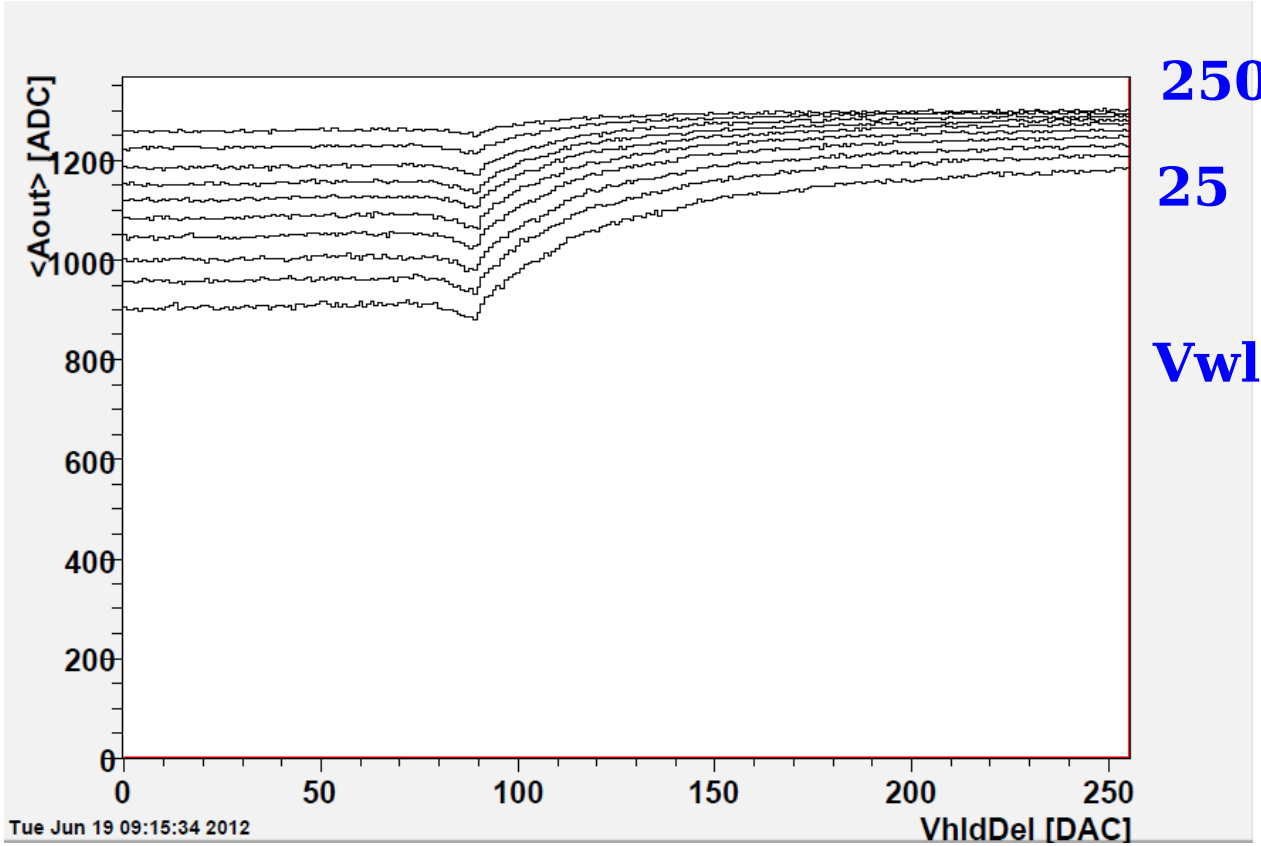
- One pixel, CtrlReg 4
- Change VwllPr from 25 to 250 with step=25. VwllSh=60, Vcal=200

Sample and hold timing xdb



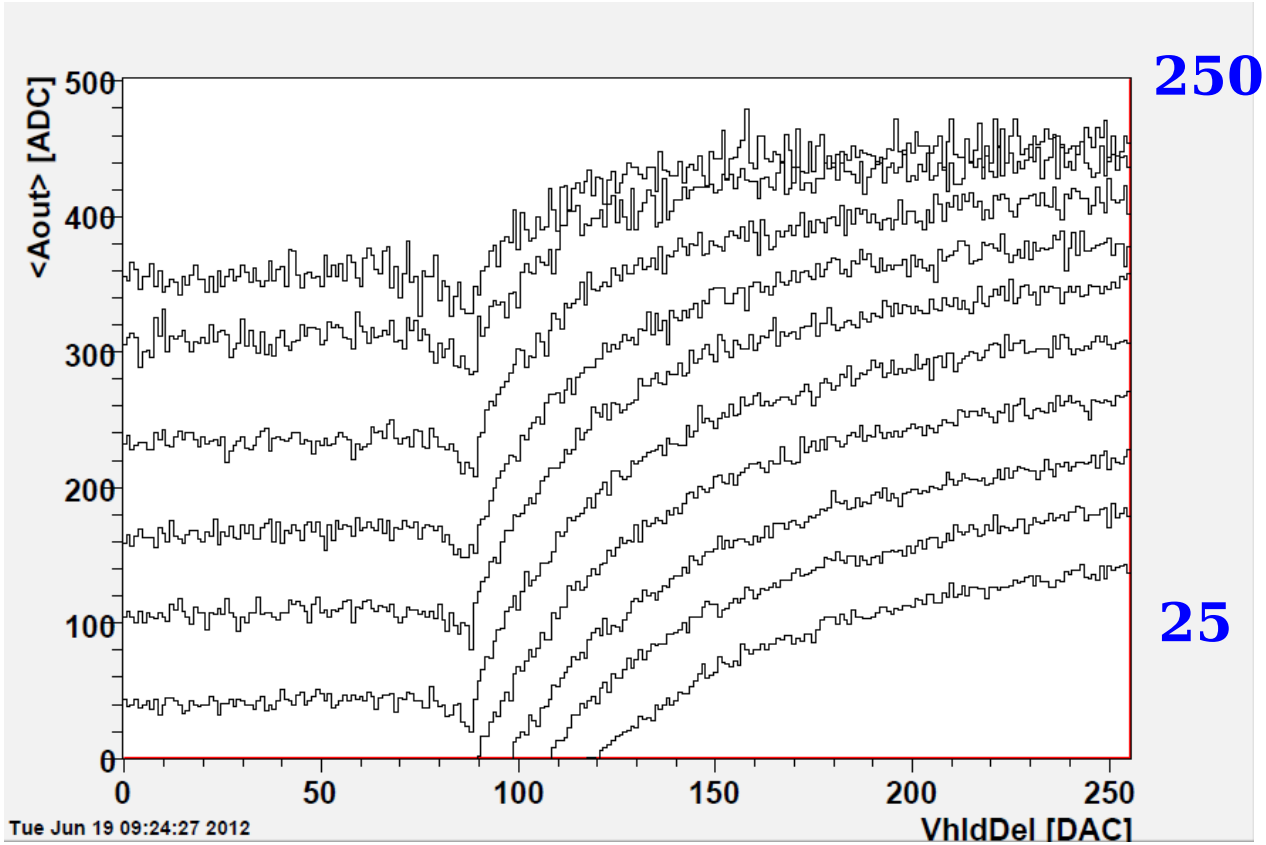
- One pixel, CtrlReg 4
- Change VwllSh from 25 to 250 with step=25. VwllPr=60, Vcal=200

Sample and hold timing xdb



- One pixel, CtrlReg 4
- Change VwllPr and VwllSh from 25 to 250 with step=25. Vcal=200

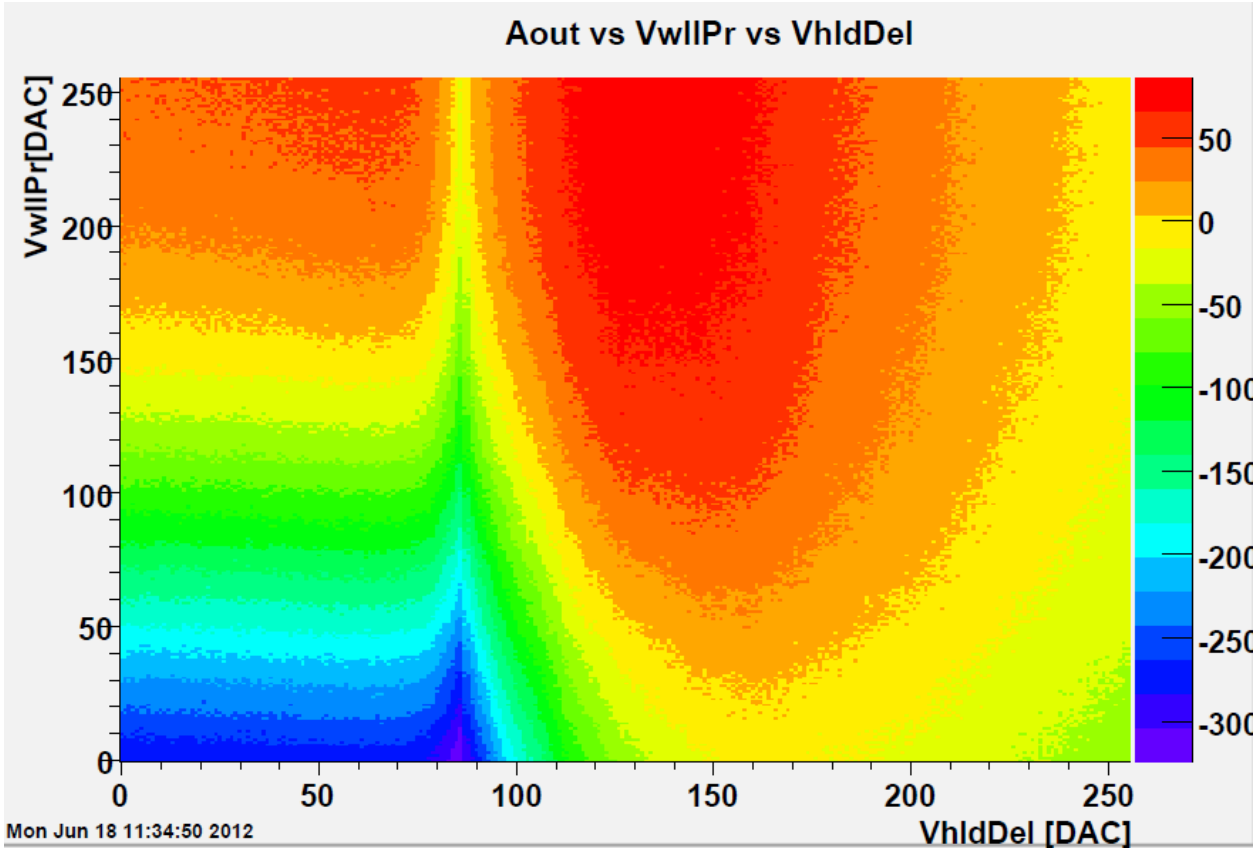
Sample and hold timing xdb



VwllSh & VwllPr

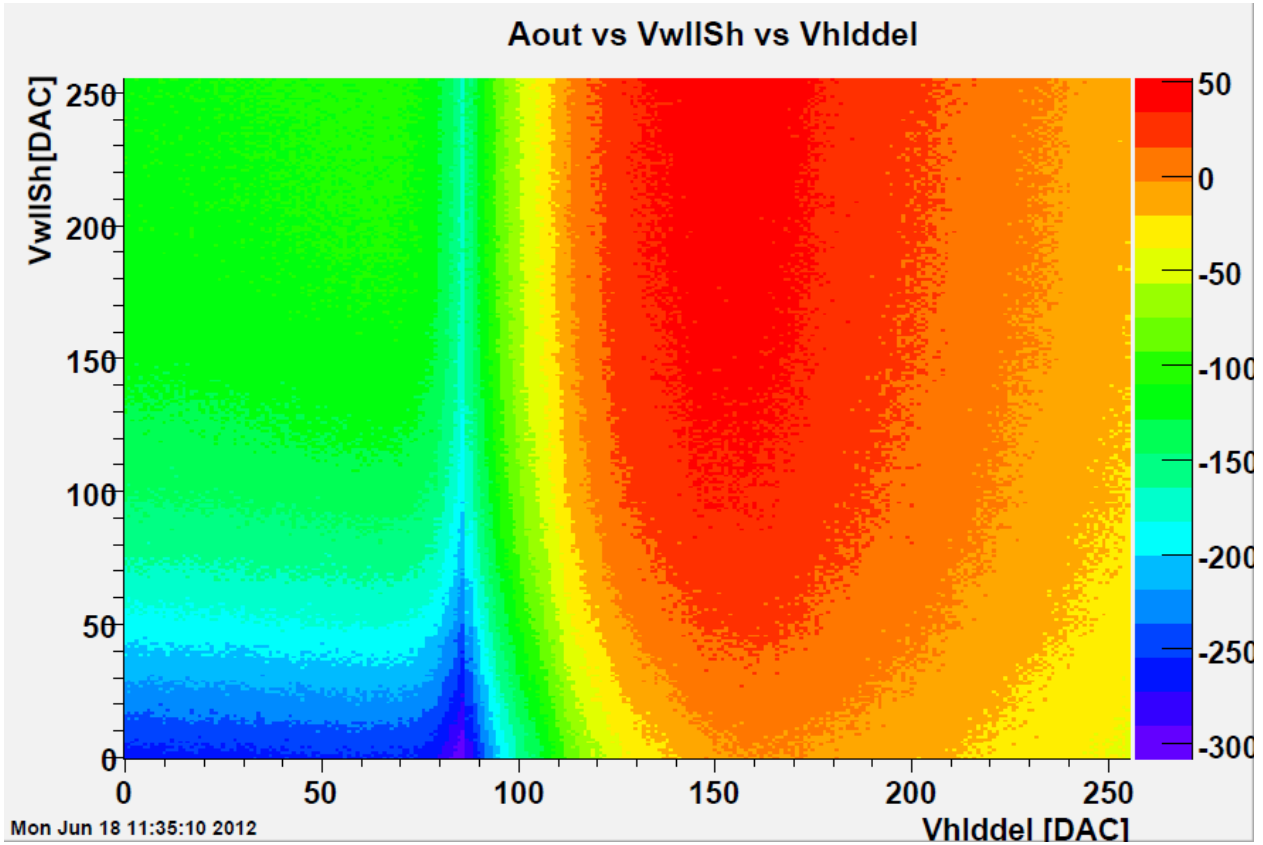
- One pixel, CtrlReg 4
- Change VwllPr and VwllSh from 25 to 250 with step=25. Vcal=50

Chip 10 CtrlReg 0



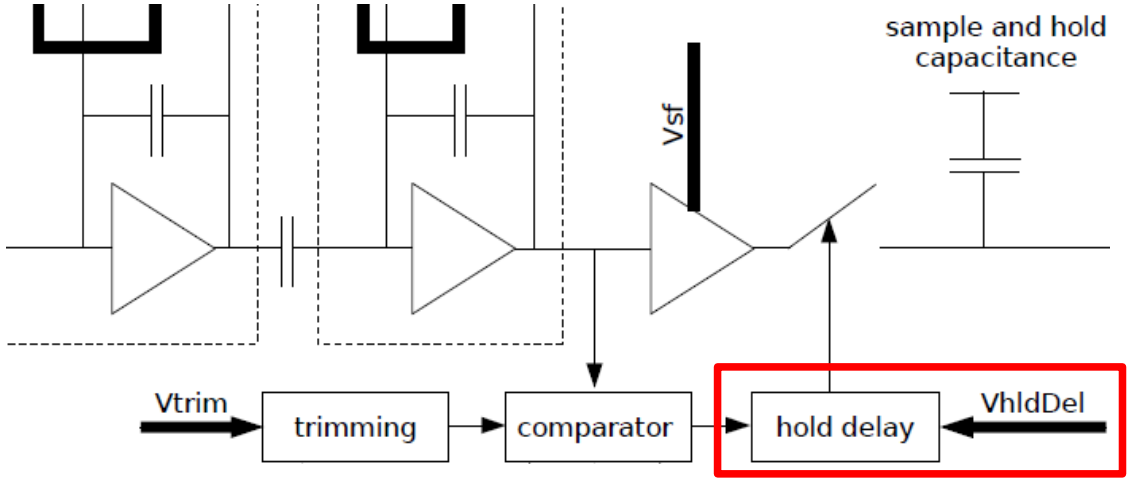
Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=35, VwllSh=35, VhldDel=162, Vcal=200, CtrlReg=0.

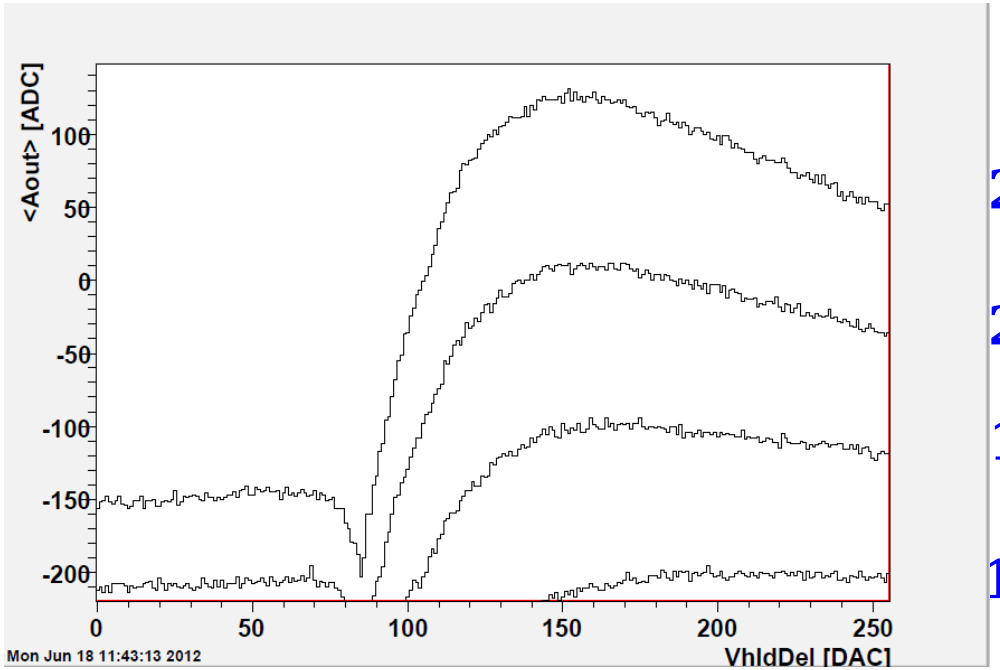
Chip 10 CtrlReg 0



Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=35, VwllSh=35, VhldDel=162, Vcal=200, CtrlReg=0.

Sample and hold timing Chip 10





250

200

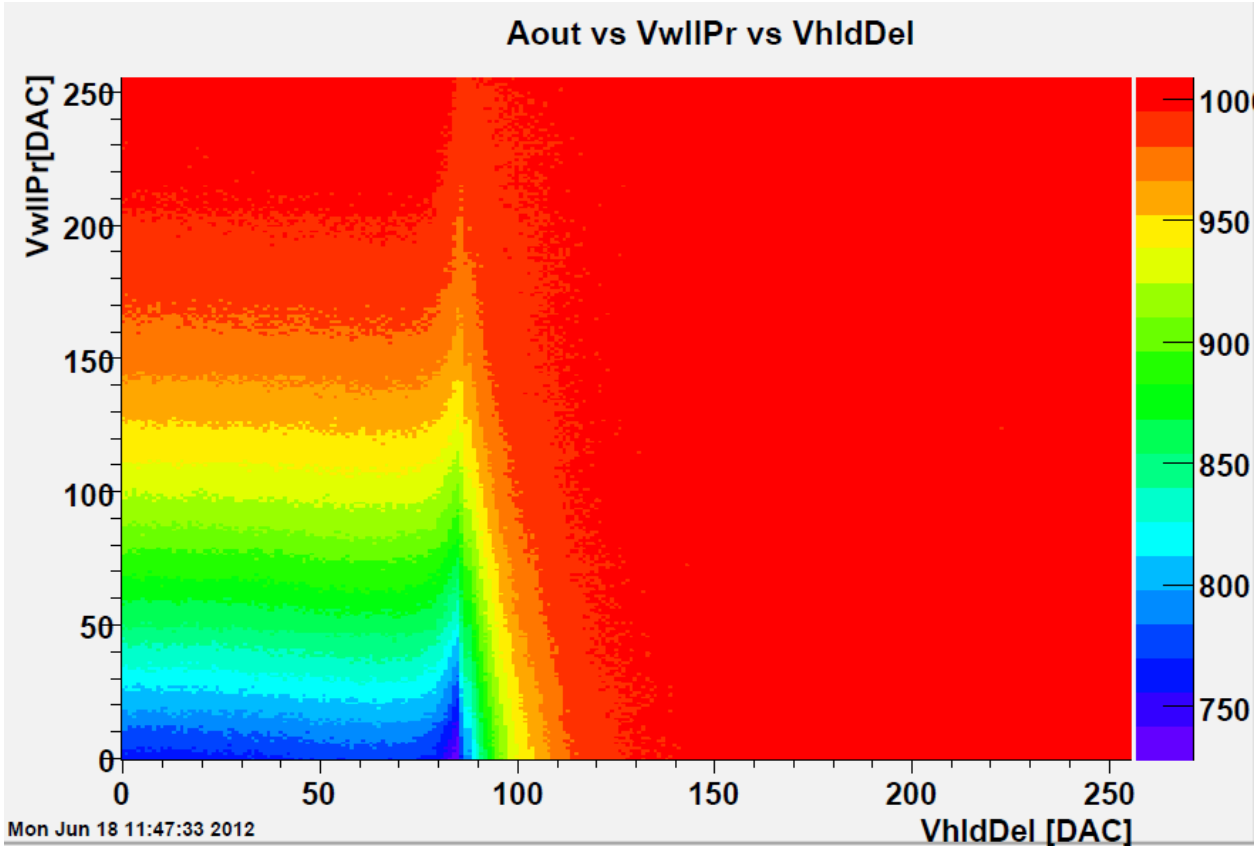
150

100

Vcal

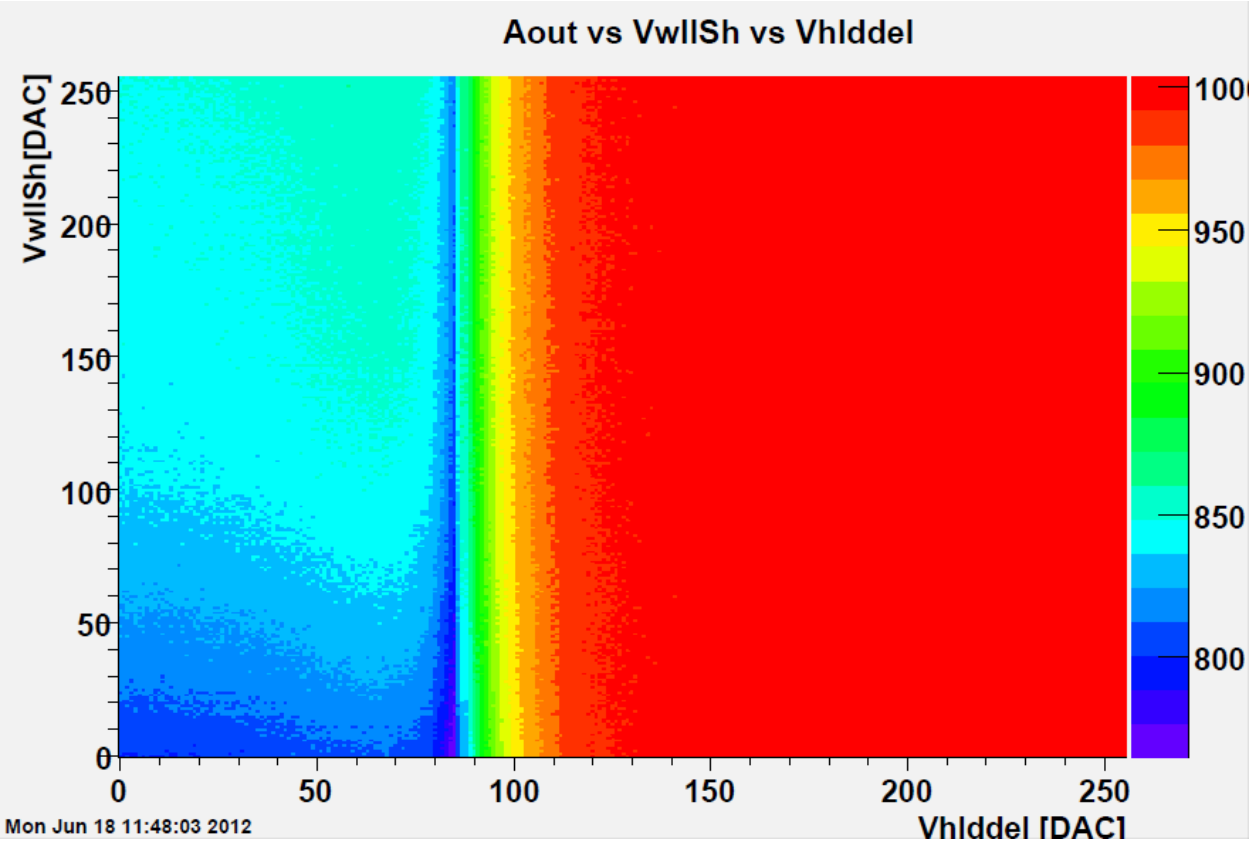
- One pixel, CtrlReg 0
- Aout vs VhldDel

Chip 10 CtrlReg 4



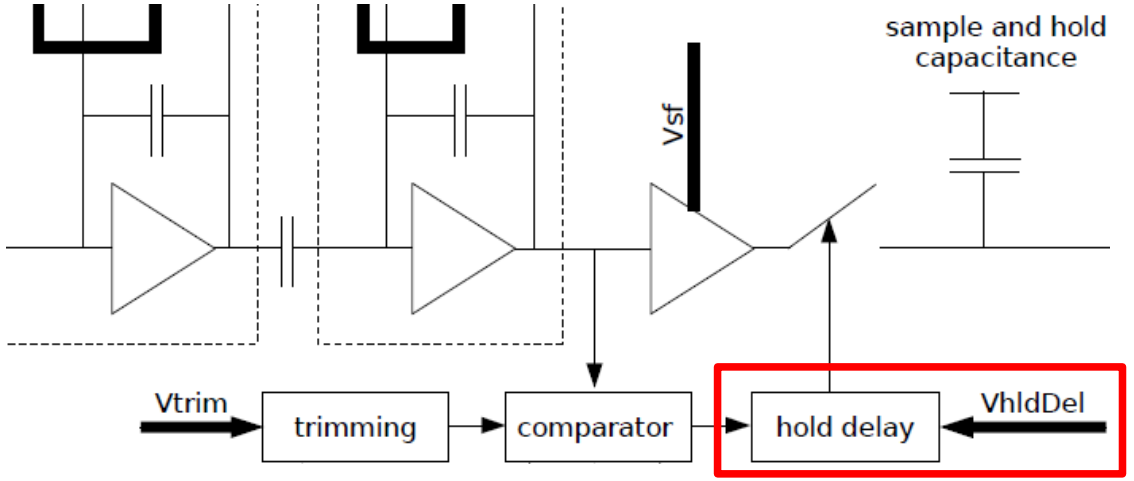
Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=35, VwllSh=35, VhldDel=162, Vcal=200.

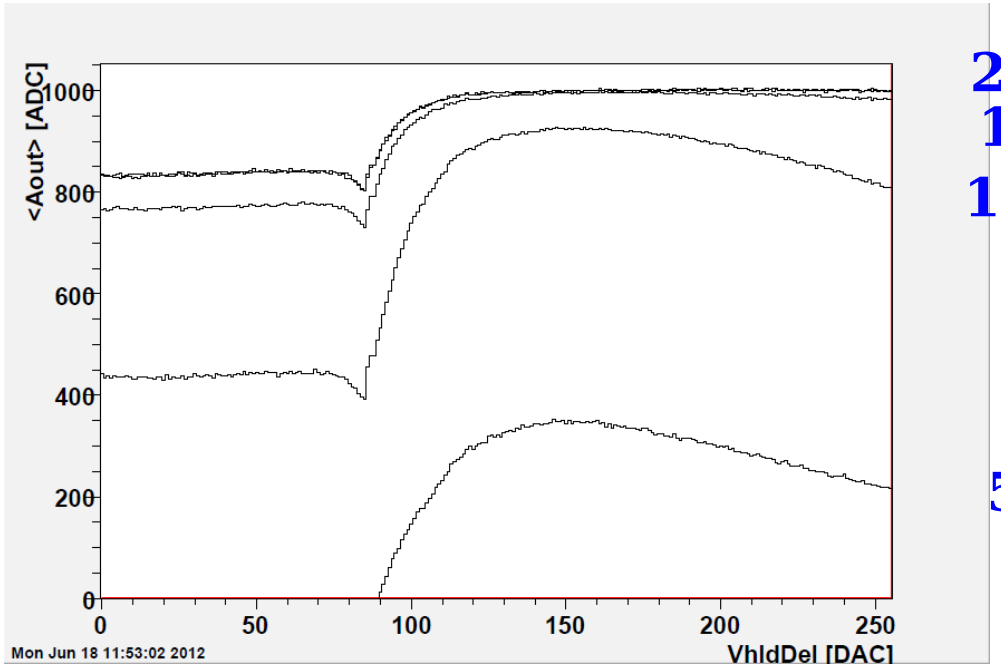
Chip 10 CtrlReg 4



Aout vs VwllPr and VhldDel. Working point at DESY: VwllPr=35, VwllSh=35, VhldDel=162, Vcal=200.

Sample and hold timing Chip 10





250/200
150
100
50
Vcal

- One pixel, CtrlReg 4
- Aout vs VhldDel

Summary

- CtrlReg 4: xdb ROC shows saturation for VhldDel DAC. ROC 10 (old type, sensor) also saturated but for high Vcal only
- Test for the xdb ROC is done with CtrlReg 4 only
- Proposal for the new working point: VwllPr=200, VwllSh=200, VhldDel=200 ?
- Working point (done with 'Pretest') is correct for both CtrlReg's for the old ROC