The CMS Hadron Calorimeter Detector Control System Upgrade

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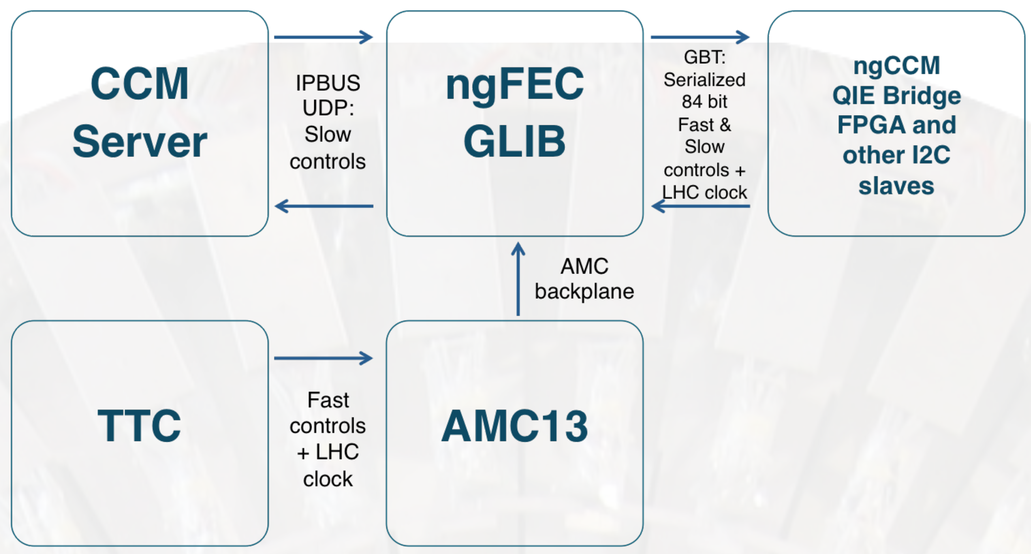
Abstract: The detector control system of the CMS hadron calorimeter provides the 40.0788 MHz LHC clock to the front end electronics and supplies synchronization signals and I²C communication. Pedestals and diagnostic bits are controlled, and temperatures and voltages are read out. SIPM temperatures are actively stabilized by temperature readback and generation of correction voltages to drive the Peltier regulation system. Overall control and interfacing to databases and experimental DAQ software is provided by the software CCM Server. We report on design and development status, and implementation schedule of this system.

Introduction

The energy and luminosity upgrade of the Large Hadron Collider (LHC) and Compact Muon Solenoid (CMS) Detector requires improvements on the CMS electronic infrastructure as well. The CMS HCAL control system is planned to be upgraded by

- replacing VME standard to µTCA which offers higher data transfer rates through the backplane, better cooling options, and power management configurations in a more compact crate;
- adding redundant control paths between the front end crates;
- improving software and firmware features, reliability, and performance.

The next generation Front-End Control (ngFEC) crate connects and organizes the control path between the front-end modules and the CMS control systems. It also distributes the LHC clock (40.0788 MHz) to the front-end readout system.



Advanced Mezzanine Card 13 (AMC13): Collects and distributes DAQ, TTC and TTS information to the modules within µTCA crate; developed by Boston University.

Gigabit Link Interface Board (GLIB): Evolution platform which provides gigabit **Small Form-factor Pluggable (SFP)** transceivers; developed by the CERN Electronics Department. The GLIB card is based on the Virtex 6 FPGA architecture.

Charge Integrating Encoder 10 (QIE10): The new version of the previous Charge Integrating Encoder (QIE8) which has been used to sum and convert analog signals to digital signals in the CMS HCAL.

Next Generation Clock Control Module (ngCCM): The clocks will be distributed to the front end modules by ngCCM. It is a replacement for the old CCM module and it is developed by UVA and CERN.

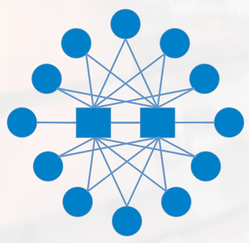
µTCA

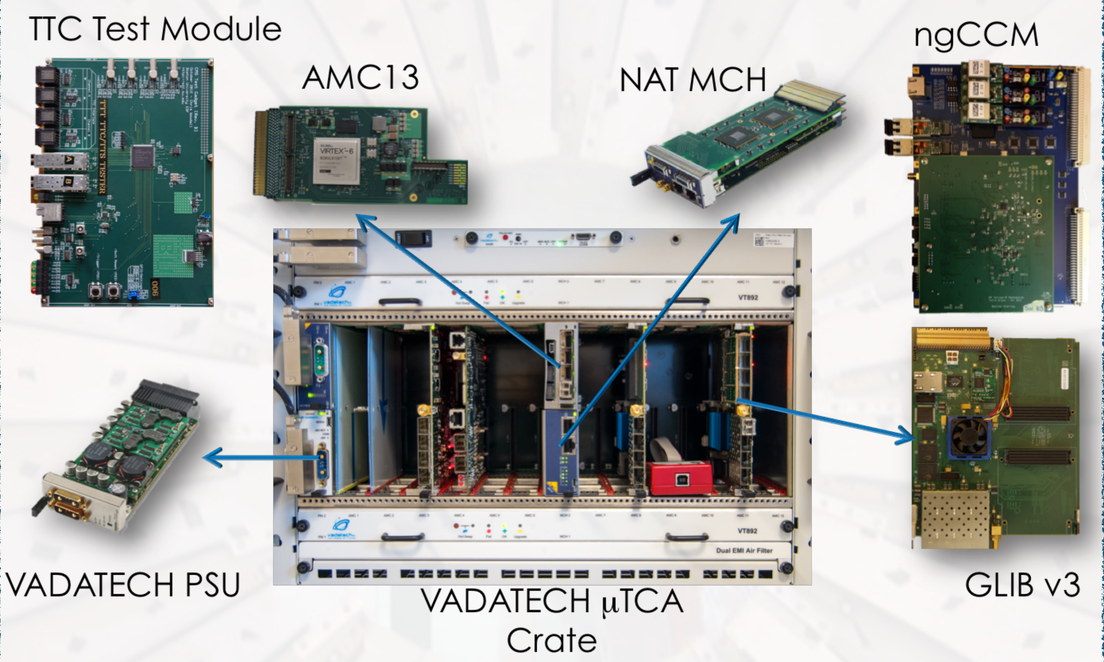
Micro Telecommunications Computing Architecture (µTCA) is a relatively new communication standard developed for handling the requirements of the next generation telecommunication and computer network equipment.

It provides some advancements over legacy standards such as:

- Better power and cooling management
- Small form factor
- Hot swapping
- Faster backplane communications

µTCA supports a dual star topology where two central hubs have connections to all other modules.





IPBUS Protocol: A reliable IP-based protocol for controlling ATCA/µTCA modules, which enables the use of UDP packets to establish the communication between the CCM Server and the ngFEC GLIB.

GigaBit Transceiver (GBT) Protocol: A transmission protocol targeting high speed data transfer in radiation-harsh environments of high energy experiments.

It provides three different encoding schemes with different error correction and detection capabilities: “GBT-frame”, “8b10b” and “Wide-Bus”. Following the different encoding schemes, the GBT protocol serializes and deserializes 120 bit frames (88 bits or 84 bits effective including slow controls) and can achieve up to 4.8 Gbit/s transfer speed.

The “GBT-Frame” encoding scheme is implemented in the ngFEC GLIB firmware.

CCM Server and TTC

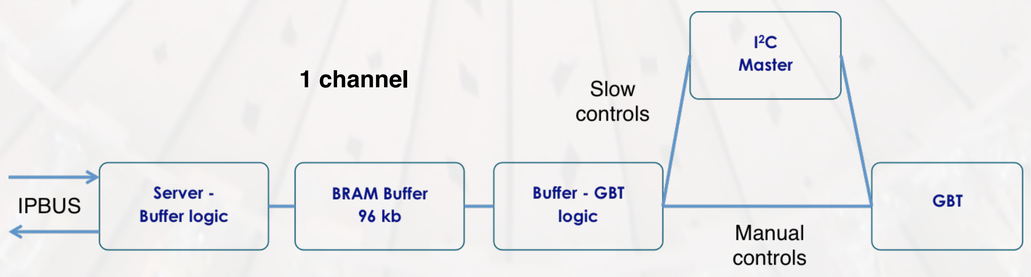
Crate Control Module (CCM) Server is developed at DESY. The CCM server sets the configuration parameters enables the front-end modules. It also reads the debugging and the sensor information (temperature, voltage etc) from the front-end modules and drives the manual controls like reset signals.

The CCM Server forms slow control commands and sends them to ngFEC GLIB board through the IPBUS protocol.

Right now, the CCM Server provides a command line interface, and a GUI will be implemented in the future as well.

The central LHC clock and fast controls delivered by the **Timing Trigger Control (TTC)** system to the AMC13 board in the ngFEC crate. The AMC13, then, recovers the fast control signals and 40.0788 MHz LHC clock from the SFP connection and distributes them to the ngFEC GLIBs.

ngFEC GLIB



One ngFEC µTCA crate is capable of controlling 672 I²C slaves on the front-end crate.

Slow control commands as well as the ngFEC GLIB specific commands received from the CCMServer are stored in dual port BRAM blocks and then processed by the ngFEC GLIB logic. The fast controls coming from TTC through the AMC13 are directly sent to ngCCM.

The ngFEC crate communicates with the ngCCM via GBT protocol through the fiber connections. One bit is reserved in the 84 bits GBT word for each I²C slave on the front-end crate. The I²C master on the ngFEC GLIB controls the bit and all the masters are sharing the same I²C clock. Therefore, even though the data transfer rate is 4.8 Gbit/s, 100 KHz I²C communication can be maintained simultaneously and independently for each front-end I²C slave.

Front-End Crate

The front-end crates are located close to the CMS detector, and mud be able to operate in the radiation-harsh environment. Therefore, the front-end modules are designed with an efficient and essential structure.

The ngCCM board distributes the fast controls commands and the LHC clock in the front-end crate and routes the slow control commands to other modules. It also has an internal I²C slave that sends temperature and status information to the CCM server.

The QIE boards carry a bridge FPGA which provides access to other components on the board (QIE, GBTx chips etc). An I²C slave is implemented on the bridge FPGA and with a custom scheme between the CCM Server and the bridge FPGA, it routes the slow control commands to other components by switching I²C lines. Therefore, with one I²C link to the QIE board, the CCM Server effectively controls all the components on the board.

Summary and Outlook

The ngFEC GLIB firmware can simultaneously drive slow controls to 14 I²C slaves and fast controls for each SFP link. There are three test stands capable of testing the control system of ngCCM: DESY, CERN and FermiLab. The CCM Server and the ngFEC GLIB firmware with two SFP links are tested in two different test stands.

Currently we are working on driving 4 and more SFP links from the ngFEC GLIB.

Links

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CMS HCAL Upgrade page

CMS HCAL ngFEC Twiki (CMS internal)

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